UNIVERSITY OF CANTERBURY

DOCTORAL THESIS

Mist-CVD deposited ZnO thin films for metal-semiconductor field effect transistors

Author:
Chikezie C.ONYEMA

Supervisor:
Prof. Roger J. REEVES

A thesis submitted in fulfillment of the requirements for the degree of Doctor of Philosophy

in the

School of Physical and Chemical Sciences

February, 2020

UNIVERSITY OF CANTERBURY

Abstract

School of Physical and Chemical Sciences

Doctor of Philosophy

Mist-CVD deposited ZnO thin films for metal-semiconductor field effect transistors

by Chikezie C.ONYEMA

ZnO is a metal oxide semiconductor that continues to attract research interests due to its desirable properties such as its direct wide bandgap, high exciton binding energy, and optical transparency. These properties make ZnO a potential material of choice for optoelectronic applications especially in the blue and UV regions of the electromagnetic spectrum. For many industrial applications of thin-film devices, a cost-effective and high throughput method for depositing good quality metal oxide thin films is crucial. This research work focusses on mist-CVD as a cost-effective method to deposit ZnO thin films at atmospheric conditions. In particular, this work adds to the existing knowledge in mist-CVD growth of ZnO films by utilizing precursors free from volatile and flammable organic solvents in the film deposition process, a recipe that is different from other reports in the literature.

Optical studies by UV-Vis transmission spectroscopy show films to be transparent, with transmission higher than 85% in the visible region and with distinct absorption edge corresponding to the onset of photon absorption by ZnO. Optical bandgap was found to lie between 3.27 - 3.32 eV depending on the thickness of films. Photoluminescence studies show dominant emission peaks at 3.362 eV and 3.321 eV near the band edge associated with donor and acceptor impurities. Crystalline properties of ZnO films deposited on different crystallographic planes of sapphire substrates indicate preferred growth orientation that is consistent with reports on epitaxial relationships between ZnO and various planes of sapphire. For growths on an r-plane sapphire substrate, the dominant diffraction peak shows preferred orientation in the a-plane ($11\bar{2}0$). The dominant diffraction peak for films grown on c-plane sapphire is along the (0002) crystal plane while for growth on an a-plane sapphire substrate, peaks from (0002) and ($10\bar{1}0$) dominate the XRD pattern. Film surface topography is influenced by growth factors including precursor concentration, temperature, and substrate type. Typical surface roughness

R_{rms} is between 2.2 nm - 4.3 nm for ZnO films deposited on an r-plane sapphire substrate at a growth temperature of 500°C with thicknesses ranging from 20 nm - 260 nm.

To demonstrate applicability of cheaply produced mist-CVD deposited films in electronic devices, ZnO films are employed as active conducting channels in metal-semiconductor field-effect transistor (MESFET) devices. Fabrication techniques involve standard photolithography and lift-off procedures. Performance characteristics of transistor devices are found to be dependent on various factors including channel thickness, physical dimensions, and choice of gate material. MESFETs fabricated with silver oxide and palladium oxide as gate electrodes exhibited excellent transistor characteristics with Schottky barrier height (SBH) approximately 1.18 eV and 0.94 eV respectively. Transistor current modulation ratio I_{on}/I_{off} as high as 10^7, subthreshold swing as low as 85 mV/decade and channel mobility >5 $cm^2/V.s$ were obtained for fabricated devices.

Under elevated temperature, ZnO-based MESFET maintains the expected field-effect transistor characteristics, though with an increase in leakage current and reduction in I_{on}/I_{off} ratio by about two orders of magnitude for a temperature increase of 25°C - 130°C. By subjecting the gate electrode of a MESFET device to positive constant voltage stress (CVS), an increase in off-state current was observed while a CVS of negative polarity has minimal effect on device functioning. Conversely, under illumination with intense UV light, transistor behavior and performance characteristics deteriorate with a break-down of the Schottky barrier, lasting several days before full recovery to the original state.

Keywords: Metal-semiconductor field-effect transistor (MESFET), Schottky Barrier, Wide bandgap Semiconductors, Photolithography.

Acknowledgements

First and foremost, I want to thank the almighty God for giving me good health, knowledge and the opportunity to undertake this research study to a successful completion. I am exceedingly thankful to my supervisor, Prof. Roger Reeves for his advice and coaching. Roger is indeed a great teacher, supporting and motivating me throughout the research project. I also thank my co-supervisor, Assoc Prof. Martin Allen for his advice and direction throughout the research project.

To the friends and colleagues that I met as part of the MacDiarmid Institute - Jonty Scott, Rodrigo Garzoni, Chrissy Emeny, Alana Salkeld, Adam Hyland, Alex Neiman, and Caixia Hou. I appreciate all the assistance, discussions and inputs you all provided in the course of this research work.

I am very appreciative of the technical expertise and suggestions provided by Rob McGregor, from the SPCS glass blowing facility. I also acknowledge the technical assistance offered by Gary Turner and Helen Devereux from the University of Canterbury Nanofabrication laboratory. I seize this opportunity to say thank you to Matt Poulson for the help you gave with X-ray diffraction measurements. I acknowledge and give credit to a former postdoctoral fellow, Giang Dang for making available his electronic chip design for use in this work.

To my wife Jecinta, you have shown great patience throughout these years. I will always be grateful for the motivating words of encouragement and acknowledge some losses you have endured as a result of years dedicated in undertaking research studies. And to my little daughter Adelle, you have given me wonderful moments of parenthood and your birth during my studies served as a source of motivation in my academic pursuit. To my parents and siblings, thank you for the support you all have provided throughout my education at all levels.

I am grateful to my employer, the University of Nigeria for facilitating the opportunity for me to carry out a Ph.D. research in New Zealand. To Christchurch community which has been my home for some years, I appreciate all the people I have met, who in one way or the other contributed to my success.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

For several decades, thin-film technology has found applications in many industrial and technological processes. It involves depositing a thin layer of material with thickness between a few nanometres to about 100 micrometers onto a substrate surface. The interest and progress that have been made in thin-film technology can be attributed to advances in electron microscopy, vacuum technology and other improvements in the equipment necessary for nano-scale material analyses. Today, thin-film deposition and the manipulation of atoms near the atomic scale constitute vital manufacturing processes utilized in the semiconductor industry enabling technologies such as thin film solar panels, LED lighting and displays, etc.

The interest in thin films stems from their many useful industrial and technological applications in addition to some of the remarkably different and unique physical and chemical properties exhibited by materials in the nanoscale which are not normally obtained in the corresponding larger-scale bulk samples. These different properties of nano-materials arise because of the reduction in spatial dimension and confinement effects in a particular crystallographic orientation which tend to lead to modifications of physical properties of the material. There is, therefore, unlimited possibilities in terms of improvement in material properties by controlling the structure and composition of materials at the very small nano-scale dimension. Research in nanotechnology has enabled the creation of desirable materials and innovations that are widely utilized across science and engineering. Metal oxide nano-structures which are transparent and conducting constitute an important aspect of nanotechnology, and have drawn the interest of scientists and engineers.

Transparent conducting oxide (TCO) are materials that show a combination of high optical transparency and electrical conductivity thereby finding applications as transparent electrodes across several optoelectronic devices. The first TCO material was developed more than a century ago which was a

thin film of CdO deposited by thermal oxidation of a vacuum sputtered cadmium metal [135]. Although Cd based TCOs exhibited the desired optical and electrical properties, the high toxicity associated with cadmium limited its use only in special applications such as CdTe/CdS thin solar cells that are highly regulated and not sold directly to consumers. Post-oxidation of evaporated metal thin films was one of the earlier methods for deposition of TCO - tin oxide (TO) was deposited in 1937 using this method [15] while an indium oxide film was reported in 1953 [192]. Over the past several decades, the most widely used and popular TCO has been tin-doped indium oxide typically called indium-tin-oxide (ITO) which is widely utilized as a transparent conductive coating for electronic displays such as liquid crystal display (LCD), flat panel and plasma displays, and touch screens. Thin films of ITO also finds its use in light-emitting diodes (LEDs), solar cells and antistatic coating. Further applications of ITO include heat-retaining windows glass and conducting electrodes for optoelectronic devices that interact with light notably as infrared reflection coatings for automotive and sodium vapor lamp glasses. ITO films are used for defrosting in aircraft windshield by applying a voltage across the film to generate heat [108, 47, 21, 198]. Despite the extended reach of ITO for a range of technological applications, reliance on indium poses a threat to global electronics as it is both expensive and not widely available. There is, therefore, a growing interest in research on indium free replacement materials and their deposition technologies.

TABLE 1.1: Comparison in the properties of Si, GaN, and ZnO

Semiconductor	Si	GaN	ZnO
Preferered crystal	diamond	wurtzite	wurtzite
Bandgap (300 K)	1.1eV (indirect)	3.40 eV (direct)	3.37 eV (direct)
Lattice constant	a = 5.430 Å	a = 3.189 Å c = 5.185 Å	a = 3.252 Å c = 5.213 Å
electron mobility ($cm^2/V.s$)	140	1000	200
hole mobility ($cm^2/V.s$)	450	5 - 50	10
Exciton binding energy	10 meV	25 meV	60 meV
Breakdown strength	3.0×10^5 V/cm	3.3×10^6 V/cm	5.0×10^6 V/cm
Melting point	1414°C	1970°C	2500°C

The present-day human lifestyle is heavily influenced by optoelectronic devices ranging from home-based appliances to multimedia and telecommunications systems which are advancing from rigid and bulky to light-weight and flexible. There is an increased desire for functionalities in optoelectronic devices which are not attained in the present-day silicon-based technologies.

Rising innovations such as smart labels, intelligent packaging, synthetic skin for robots, transient medical implants in addition to advanced surgical tools require electronic devices to be miniaturized, flexible and transparent. These requirements can be fulfilled by thin-film transistors (TFTs) which are increasingly studied by researchers. TFTs based on transparent metal oxide are particularly desired owing to their optical transparency, good electrical performance in addition to good mechanical properties - resistant to strain and ability to be bent up to 25 μm radii [203, 178, 100, 81]. Today, TFTs are used as pixel switching elements in flat panel displays for which metal oxide TFT materials such as ZnO are continuously making steady progress in digital display technologies. Further, metal oxide TFTs are challenging the dominance of silicon in conventional application and opening opportunities for transparent displays [29, 182].

Zinc oxide (ZnO) has gained considerable research focus as a potential replacement for ITO. It is a group II-VI compound semiconductor material with a direct bandgap of $\approx$ 3.37 eV at room temperature making it transparent to visible light. The bandgap of ZnO makes it a desirable materials for LEDS, laser diodes and photodetectors that operate in the blue to UV wavelengths. ZnO has been studied over several decades due to its promising properties for UV/blue optoelectronics, transparent electronics, spintronics devices, and gas sensing. With its optical transmittance in the visible region typically above 80% and low electrical resistivity ($< 10^{-3}\Omega-$cm), ZnO films serve as a promising candidate for applications involving TCOs in device fabrications.

Perhaps, one can point to one of many reasons for the renewed research interest in ZnO by considering the technological revolution brought by gallium nitride (GaN). GaN is a binary direct bandgap semiconductor and shares similar optical and crystalline properties with ZnO as represented in Table 1.1. Both GaN and ZnO show similarities in their crystal structure, bandgap, the lattice constant, etc. In addition to several optoelectronic applications of GaN, its use in the GaN-based light-emitting diodes (LEDs) is quite significant enabling light emission spanning from red to the ultraviolet by doping with either aluminum (AlGaN) or indium (InGaN) with the bandgap depending on the ratio of In or Al dopant [151]. This attractive feature to tune the bandgap of GaN enables light emission in the complete range of visible spectrum using GaN-based LEDs thus, full-color light sources and blue LED devices can be fabricated. This feature is also displayed by ZnO. The bandgap energy of ZnO can be tuned to $\approx$3.0 eV by doping with Cd while

Mg increases the bandgap energy to ≈ 4.0 eV [94].

ZnO has an exciton binding energy of ≈ 60 meV, as compared to GaN ≈ 25 meV. This added advantage over GaN implies a greater room temperature luminescence efficiency. The excitonic binding energy quantifies the strength of the bond between the bound electron and hole pair (exciton) and thus, the higher the exciton binding energy, the less likely for excitonic dissociation through thermal effects.

The room temperature Hall mobility for a single crystal of ZnO is ≈ 200 cm^2V^{-1} which is lower than that of GaN, but ZnO has a higher saturation velocity. Further, ZnO shows improved resistance to radiation than GaN and can have a possible application in space and nuclear applications. Good quality single crystals of ZnO are also available [173]. The crystal growth of ZnO is also less complicated which could enable less expensive engineering of ZnO-based devices. Furthermore, ZnO is adaptable to wet and dry etching [190, 149], the desired property for device engineering and fabrication.

A number of deposition methods are employed for the growth of ZnO and related oxide materials. Pulse laser deposition (PLD) [253], molecular beam epitaxy (MBE) [118], magnetron sputtering [25], chemical vapour deposition (CVD) [101], metal-organic chemical vapor deposition (MOCVD) [98] have all been extensively used for growth of ZnO thin films in recent times. Also, solution-based chemical methods such as sol-gel [162], hydrothermal [168] and electrochemical deposition [64] methods have been reported for the growth of ZnO thin films. Whilst MBE, MOCVD, and PLD are known to produce crystalline films of high quality, these techniques are relatively non-economical and complicated. The requirement for a vacuum system makes these methods expensive for large scale deposition and fabrication of devices. As for the RF sputtering technique for film deposition, low deposition rate, high equipment cost and the relatively high cost of ceramic target materials motivated the development of alternative growth processes. In addition, sputtering could be affected by high energy species in the plasma which can induce defect in the film or cause substrate damage [90]. In recent years, the popularity of sol-gel methods comprising of techniques such as spin coating [162], dip coating [221], spray pyrolysis [206] and mist-CVD have increased mainly due to the simplicity and cost-effectiveness of these methods. Low cost, high throughput, and large area coverage are some of the desirable features that are expected from solution-processed growth methods which are becoming increasingly popular.

The desire for industrial-scale high throughput and low-cost deposition

of ZnO have led to the development of atmospheric vapor based growth techniques that can be operated continuously without the need for vacuum systems. For instance, high production throughput and a large area deposition are required for solar cell manufacturing. The mist chemical vapor deposition (mist-CVD) is one of such cost-effective growth techniques for oxide thin film that utilizes non-toxic metal sources for the film deposition at atmospheric conditions.

As noted previously, transparent conducting oxide find applications across several technological processes and electronic devices. The key aspect of the work presented in this thesis is to show that good quality ZnO film can be deposited on substrates using a cost-effective mist-CVD growth process. Further, the deposited films are applied as active conducting channels in the fabrication of electronic devices as metal-semiconductor field effect transistors (MESFET).

1.1 Wide bandgap electronics

Silicon-based electronics have dominated the whole of the 20th Century and may still remain ubiquitous in the coming decades. However, as the need for additional performance and stability in power electronics increases, that dominance is beginning to erode as engineers are continually looking towards wide bandgap semiconductors (WBG) for the next generation of optoelectronic devices. They are so-called because of the relatively higher energy bandgap of between 2 - 4 eV [245] compared with silicon. Wide bandgap semiconductors offer some advantages over silicon including faster switching speed, carrier mobility in addition to a good number of them having a direct bandgap. The requirement in blue/UV light photonics, transparent electronics, and stability for high power and high-temperature devices are beyond the limits of silicon.

Semiconductor materials with wide bandgap energy offer less leakage current and improved dielectric strength which are important properties for high power and high-temperature electronics. The two most popular WBG semiconductor materials with a well-established technological application are silicon carbide (SiC) and gallium nitride (GaN). While silicon has a bandgap energy of 1.1 eV, the bandgap energy of SiC and GaN is 3.3 eV and 3.4 eV respectively. SiC is widely applied across several power devices and offers some advantages over silicon including reduced power losses, higher switching frequency and up to a three-fold increase in thermal conductivity

[239]. SiC is comparably more expensive to produce than silicon leading to GaN-based devices as an alternative for application in power and radiofrequency devices. As earlier noted, the technological leap ushered in by GaN

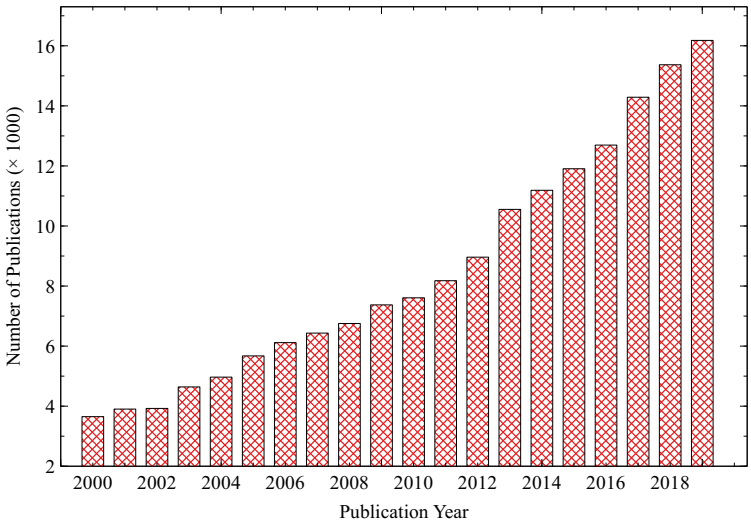


FIGURE 1.1: Annual growth in the number of publications relating to ZnO semiconductor material as obtained from ScienceDirect.

has been a motivating factor towards the renewed interest in ZnO among researchers. As can be observed in the chart of Fig. 1.1, there has been a steady increase in publications relating to ZnO over the past 20 years. The similarities in the properties between ZnO and GaN make it a notable potential material for wide bandgap power electronics and other optoelectronic applications amidst other added advantages relating to its exciton binding energy. It has already been mentioned that the higher exciton binding energy of ZnO potentially puts it as a more efficient luminescent material than GaN. Also, ZnO shows varied growth morphologies where different orientations of nanostructures can be formed. Nanostructures of ZnO such as nanowires, nanorods, nanoplates, nanobelts, nanocages can be formed and used in device fabrications which can be potentially utilized in optoelectronics, gas sensors, and transducers [236].

One of the limiting reasons that have constrained optoelectronic applications using ZnO is the difficulty associated with having a stable and reliable method of p-type doping in ZnO. However, there are opportunities for applications in uni-polar devices using its intrinsic n-type conductivity such as in Schottky based devices including diodes and field-effect transistors. Even though the charge carrier mobility of amorphous silicon is lower than in ZnO

by about 2 orders of magnitude, amorphous silicon has been the standard material of choice for pixel switching in flat panel display technologies.

1.2 General aims and thesis layout

The research project undertaken at the University of Canterbury mainly focusses on the growth of ZnO films using the mist-CVD deposition methods and application of the films in microelectronic transistor devices. Mist-CVD is a film deposition technique that is cheaper compared with vacuum-based methods such as PLD or MBE. There is a potential economic benefit if the mist-CVD deposition method can be used to produce good quality ZnO films suitable for applications in optoelectronics. Further, the deposition method offers a quick and cost-effective means of investigating film growth of various material composition especially oxide materials. As it does not require vacuum system, the financial cost of acquiring and running such system is eliminated. There is also the technique merit that potentially allows for an easy upscaling of the growth system to allow for a less cumbersome way of depositing of multi-layer material structures.

The work presented in this thesis was carried out at the Department of Physics, and Nano-fabrication laboratories within the Department of Electrical and Computer Engineering, University of Canterbury, New Zealand. The research project has the following aims:

- To develop an efficient and economical way to deposit ZnO based thin films using the mist-CVD film deposition technique.
- To characterize and study the properties of these films including their electrical, optical, morphological and structural properties.
- To investigate the performance of deposited films when used as active channel layers in thin-film transistor devices.

In the layout of this thesis, the introductory chapter has briefly presented some of the interesting properties of ZnO as a wide bandgap semiconductor material. A discussion of some of the beneficial advantages that WBG semiconductors such as ZnO could bring to power electronics and photonics applications in the blue and UV region have been presented. In Chapter 2, the literature is reviewed to give a general background knowledge of some of the existing thin-film deposition techniques with a further theoretical outline on band structure, crystal structure and optical properties of ZnO.

Chapter 3 describes the mist-CVD system for the growth of thin films and outlines some of the motivating reasons for the choice of the growth technique as opposed to other deposition methods. There is a discussion on a number of characterization methods used to investigate crystalline structure, surface morphology, optical and electrical properties of deposited thin layers of ZnO films on various substrates. Chapter 4 presents the results on the growth of ZnO films and investigates how some of the growth parameters affect the properties of the film.

Chapter 5 is devoted to a discussion on the optical properties of ZnO films as investigated from two optical spectroscopic techniques - transmission spectroscopy in the UV-Vis region to study light absorption/transmission and photoluminescence spectroscopy which gives the luminescence properties of deposited ZnO film. In Chapter 6, the discussion focuses on the physical principles behind a Schottky barrier and its application in metal-semiconductor field-effect transistors (MESFET) to control the current flowing through such a device. Additionally, a discussion of the experimental steps taken in the fabrication processes of a micron-sized MESFET is presented including characterization setup to assess transistor performance.

The discussions in Chapter 7 focuses on the performance of fabricated MESFETs that utilized samples of mist-CVD deposited ZnO films as active channel. It presents results and the effects of factors such as physical dimensions, film thickness and gate material transistor performance. Further, the stability in the performance metrics of transistors under conditions such as voltage bias, elevated temperature, and UV illumination are investigated with results presented.

The concluding Chapter 8 gives an overview of what has been learned as part of the research project and outlines areas where further work and improvement will be needed in relation to the mist-CVD growth of ZnO films and applications for electronic devices.

Chapter 2

Literature Review

2.1 Introduction

This chapter is devoted to reviewing some of the available thin film deposition technologies and their basic operational principles. An overview of the band theory of solids is presented. Further, the chapter discusses a theoretical background on some of the important properties of ZnO including its optical and crystalline properties in addition to the origin of its intrinsic conductivity.

2.2 Thin Film Deposition Methods

Film deposition on a surface can be achieved either through physical or chemical vapor depositions. The physical vapor deposition methods comprise vacuum-based techniques in which desired materials to be deposited transforms from a solid phase to a vapor phase and condenses on a substrate [185]. PVD techniques are generally vaporization based thin film coating methods that transfer materials at the atomic level without any chemical reaction occurring during the deposition process. Three fundamental steps in PVD methods encompass vaporization of solid target materials which can be assisted by high temperature or gaseous plasma, transportation of target vapor and finally, the condensation of the vaporized material on the substrate to form a film. The common PVD methods include sputtering and thermal evaporation.

Chemical vapor deposition (CVD) techniques consist of methods that involve the use of a chemical process to produce thin films and are widely used in the semiconductor industry. In its basic principle, CVD growth techniques employ precursor chemical which reacts or decompose on the substrate to form thin films of the desired material. Most of the time, volatile

by-products of chemical reactions are produced in CVD processes which are normally eliminated through gas flow within the reactor.

In this section, an overview of some of these thin film deposition techniques that are widely used for the deposition of thin layers of materials is presented. Most of the thin film deposition methods that will be described are available facilities at the laboratories that I carried out my research and gained a substantial level of knowledge on their working principles and techniques.

2.2.1 Thermal Evaporation

Thermal evaporation is one of the simplest physical vapor deposition techniques in terms of its working principle. The technique allows a thin film to be deposited by heating a material above its melting point in a vacuum chamber until the surface atoms gain sufficient kinetic energy to eject from the surface. A substrate placed above the evaporating surface is coated by the thermally evaporated materials. Thermal evaporation is commonly used for depositing metals with modest melting points such as silver, nickel and chrome, titanium and gold. Deposition parameters such as material source temperature, pressures, evaporation time and substrate type affect film properties and need to be selected properly. The source temperature of the material to be deposited is determined by its volatility.

For efficient film deposition, the pressure in the evacuated chamber will have to be sufficiently low for the free-mean-path (average distance traveled before the collision) of the evaporated molecules to be greater than the average distance of travel between the source and the substrate typically between 25 - 70 cm. At 10^{-5} Torr, the mean free path is about 5 m and significantly reduces to about 0.5 m at 10^{-4} Torr [145]. The long mean free path enables the evaporated atomic species to travel in straight lines and deposit thin layers of films on the substrate/wafers.

The material to be vaporized is loaded in a heated crucible which can be achieved through different heating systems: resistive, inductive, and electron beam evaporators. The resistive heating system is done by passing current through a resistive wire of low vapor pressure (e.g. tungsten) embedded in the crucible. For induction heated systems, RF power from an induction heating coil surrounding the source metal is used to achieve evaporation.

The electron beam evaporator relies on intense and high energy electron

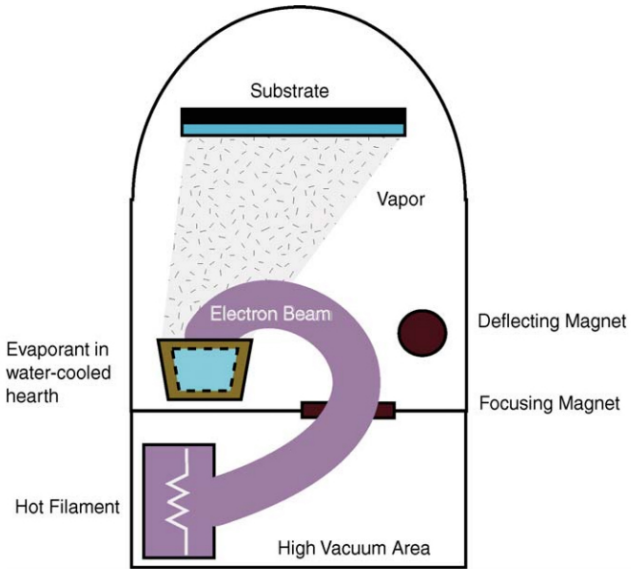


FIGURE 2.1: Schematic diagram of an electron beam evaporator. Image courtesy of MTS [49]

beam produced through thermionic emission from a filament (typically tungsten). The electron source is placed in a location outside of the deposition zone to minimize contamination from the filament. The electron beam is directed via the magnetic field into the material to be evaporated. The kinetic energy of the bombarding electron is transformed to heat on impact with the source metal raising its temperature. At low vacuum pressure and sufficiently high temperature, vapor from the source metal will be formed which then coats the substrate/wafer with a thin film of the material. The schematic diagram of an electron beam evaporation system is shown in Fig. 2.1. Some research papers on ZnO film deposited through thermal evaporation techniques are available [55, 92, 144, 1]. Ma *et al.* reported the deposition of Al-doped, transparent and conducting ZnO film on a heated glass substrate by thermal evaporation of zinc acetate and aluminum chloride in vacuum [144]. In the report of Ref. [55], polycrystalline ZnO films with thickness ranging from 10 - 80 nm were deposited using zinc target on silicon substrates. Aghamalyan *et al.* [1] reported a c-axis oriented ZnO film deposited on a sapphire substrate using an electron beam evaporation technique with optical bandgap found to be between 3.27 - 3.30 eV.

The electron beam evaporator was widely used for depositing thin films of Ti and Au contact electrodes in the fabrication process of microelectronic MESFETs with ZnO films as the active conducting layer as discussed in Chapters 7 and 8.

2.2.2 Sputtering Techniques

Sputtering is a physical vapor and vacuum-based technique that is commonly used to deposit thin films of different materials. In a sputtering process, the target material, substrate, and the electrodes are kept in a vacuum chamber. An inert gas such as argon, neon or krypton (depending on the nature of the target material) is introduced into the chamber. Passing an energetic wave through the inert gas in a vacuum causes ionization of gas forming high energy plasma ions. The target material (cathode) is then bombarded with these energetic positive ions leading to the ejection of atoms from the target (sputtering) via energy and momentum transfer.

Sputtering is a widely used thin film deposition technique that finds applications in the semiconductor industry. It is used in the deposition of metals and also for insulating materials. Sputtering offers some advantages over thermal evaporation. Sputter film deposition produces high energy flux with high surface mobility and can form films that are smooth, dense and continuous better than thermal evaporation [199].

DC Diode sputtering

In its basic design, the DC diode comprises two electrodes enclosed in a vacuum chamber and a power supply. The cathode or the target material is kept at a negative potential while the substrate to be coated (anode) is maintained at positive charge bias [237]. Sputtering gas typically argon is introduced into the chamber at millitorr pressure range with the application of a voltage between the plates. Depending on chamber pressure, sputtering gas and cathode material, plasma discharge of positively charged ionized gas atoms occur above the threshold breakdown voltage. A plasma is a weakly charged hot gas-like state of matter comprising of gas ions and electrons that gives the visible plasma glow. Positive ions typically Ar^{+}, bombard the negatively charged cathode ejecting mostly neutral atoms of the target material which eventually condense on the substrate. In the DC sputtering process, most of the energy of the bombarding ions on the target material results in heating requiring the need for cooling systems.

Even though the DC diode sputtering is simple in its operating principle, it could suffer from low deposition rates arising from low plasma densities, high gas densities, high discharge voltage and lack flexibility in terms of the choice of target material [21]. DC sputtering as a cost-effective method can only be used to deposit conductive materials such as gold. Even for the

growth of insulating films through reactive sputtering of conductive targets, the formation of an insulating layer on the target and poisoning of the target limits its use and versatility for film deposition [199].

Radio-frequency Sputtering

The RF overcomes some of the limitations of the DC sputtering and provides a means of depositing both conducting and insulating films. An RF frequency typically 13.56 MHz or some multiples is linked to the target material through an impedance network. The alternating RF power which is coupled to the electron motion in the plasma leads to increased ionization from the collision and higher plasma densities [199]. With RF sputtering, insulating materials such as silicon dioxide and alumina can be deposited since the alternating polarity of the target cathode forbids the build-up of charges on the cathode surface. Almost all metal elements can be deposited through RF sputtering.

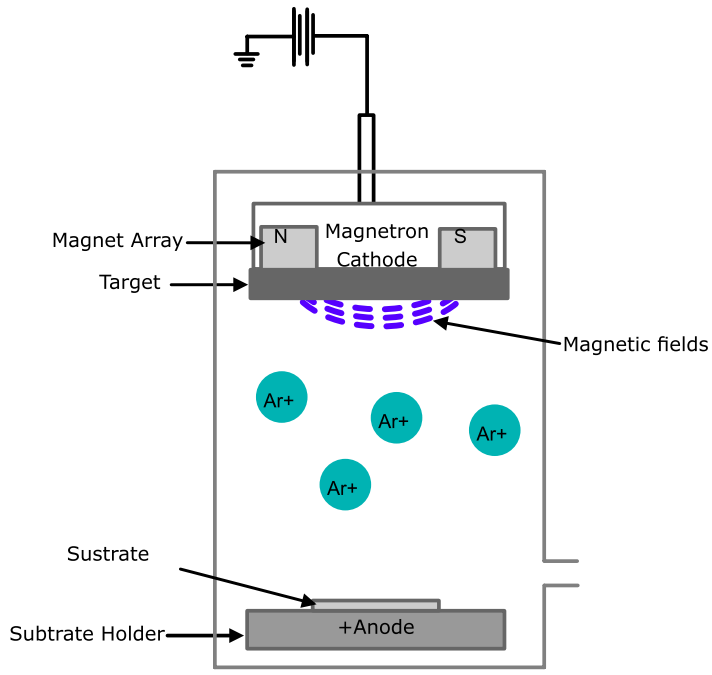


FIGURE 2.2: Schematic representation of a magnetron RF sputtering system for the growth of thin films.

The RF magnetron sputtering technique employs a magnetic field that is transverse to the electric field at the surface of the target which produces a critical modification advantageous to the sputtering process. The magnetic field enables trapping of the secondary electrons generated by the target

which will otherwise contribute to increased substrate temperature and radiation damage. The magnetron sputtering technique, therefore, allows the growth of thin films on surface sensitive or temperature-sensitive substrates such as plastics with minimal damage on the substrate. Further, magnetron sputtering improves deposition rate compared with conventional sputtering targets and can, therefore, be a relatively economical method for large scale and industrial film deposition.

ZnO films grown using sputtering are widely investigated in several research articles with a few of them listed in these Refs [10, 152, 25, 61], due to its simplicity and capacity to deposit films at low temperature. Typical growth condition is done at room temperature with pure Ar/ O_2 as sputter gas and process pressure approximately $10^{-3} - 10^{-2}$ torr. Reactive sputtering can also be used for ZnO film growth with O_2 and Ar as reactive and sputtering gases respectively. In the course of my work, RF sputtering was the deposition method of choice for oxidized metal Schottky contacts such as AgO_x, PdO_x, IrO_x and PtO_x in the fabrication process of MESFETs discussed in subsequent chapters.

2.2.3 Pulsed Laser Deposition

The pulsed laser deposition (PLD) is another of the physical vapor methods for thin films. In the basic configuration of a PLD system, a focussed, high power laser beam positioned outside of the vacuum chamber is used to strike a target of desired material composition causing the material to ablate/vaporize and deposit as a thin film on a substrate opposite the target. This is typically done in a highly evacuated environment or with a process gas in the vacuum chamber e.g. oxygen gas for the growth of oxide films. The laser beam is focussed on the target surface through external lenses. PLD first came into prominence in 1987 when a thin film of high critical temperature superconductor $YBa_2Cu_3O_{7-x}$ - (YBCO) was grown using the technique. The PLD technique is one of the most practical methods to obtain films of complicated material composition such as multi-component oxide materials. It is extensively used to fabricate films of copper oxide superconductors, ferroelectric and ferromagnetic oxides [79].

The basic set-up of a PLD system is shown in Fig. 2.3. It consists of a vacuum chamber, a substrate holder with temperature controllable heaters. Most of the non-metallic materials that are commonly ablated, have strong light absorption at the UV range around 200 - 400 nm. An excimer laser pro-

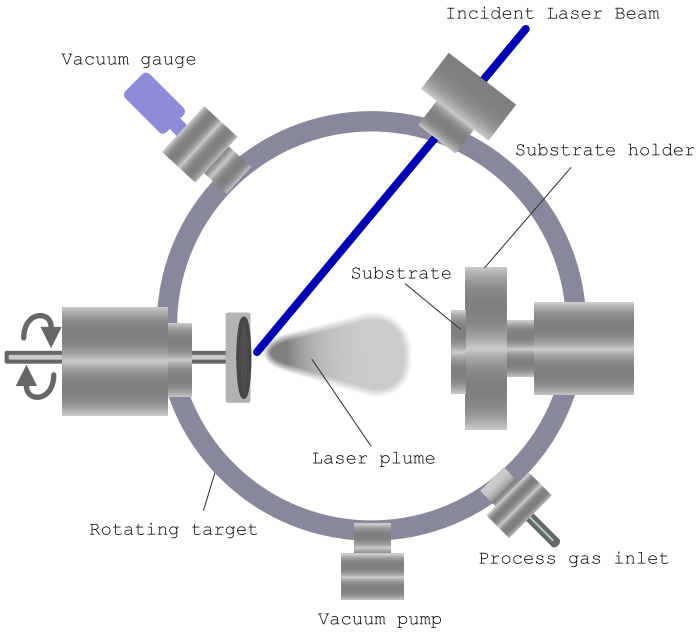


FIGURE 2.3: Schematic representation of the PLD system for growth of thin layers of a material on a substrate.

duces pulses with wavelengths in the UV region. The laser pulse is focussed through lenses and mirrors onto a solid target. The fluence of the laser can be controlled by varying the laser output energy or the focusing optics. The target material is typically a sintered ceramic with the material composition of the film to be deposited. Depending on the properties of the target material, laser energy, and pulse duration, the ablation of target material occurs above a threshold energy density. The ablated material forms an ablation plume directed towards the substrate placed at a distance of 4-8 cm and re-condenses to form films. Growth of ZnO using PLD are well reported in the literature [253, 207, 159]. Epitaxial growth of ZnO film was achieved on sapphire substrates using the PLD technique at deposition temperatures of 500 - 800°C [207]. Similarly, Muth *et al.* [159] reported growth of ZnO thin films on sapphire substrates and found that annealing the films in oxygen dramatically improved the optical and electrical properties.

2.2.4 Molecular Beam Epitaxy

Molecular beam epitaxy (MBE) is a technique used to deposit epitaxial (i.e. layer by layer) thin films of target materials of superior quality on a substrate. It can be used to deposit films of oxide materials, semiconductors, metals, and insulators [7, 17] with the ability to control film growth at a mono-layer

level. MBE is applied in the commercial fabrication of special semiconductors used in the optoelectronics and high-frequency devices. There is the requirement of ultra-high vacuum (UHV) environment in the growth of films using MBE which ensures that a very pure form of the desired crystal is grown. The ultra-high vacuum environment also enables the beam pressure to be efficiently controlled.

In the MBE, a material is sublimated or evaporated (for a liquid source) from the effusion cells, forming a molecular beam. The effusion cell is made of crucible containing the source material which is heated via ohmic heating using a filament wound around the crucible or by electron heating. The quality of growth in an MBE is dependent on the arrival of atoms on the surface and is very sensitive to impurity atoms such as nitrogen and oxygen [27]. The thermal molecular beams move in the ultra-high vacuum chamber and interact at the surface of a heated substrate to diffuse and form an epitaxial layer of film. Though its principle of film deposition is simple, several complex technologies are involved to ensure controllability and that films of desired purity and uniformity are grown. Investigation on ZnO films deposited through the MBE process and their properties are reported in the following Refs. [167, 11, 12]. In the report of Ohgaki *et al* [167], ZnO films were grown on sapphire substrate by MBE under oxygen radical irradiation. It was found that the growth rate was dependent on the Zn flux with carrier mobility of up to 42 $cm^2/V.s$ found for the films. Charge carrier concentration was between $\sim 10^{-18}$ - 10^{19} and was dependent on the substrate temperature, decreasing with increase in the temperature.

The MBE has increasingly become the standard growth method for best quality films for which other methods of growth are compared to it. While it has been applied commercially, the MBE suffers from low yield resulting from low growth rate when mass production of films is desired compared with other techniques such as Liquid Phase Epitaxy (LPE) and Metalorganic Chemical Vapour Deposition (MOCVD).

2.3 Chemical Vapour Deposition

The CVD methods allow for film growth by the chemical reaction of the precursors in the vapor phase. The requirement for chemical reaction differentiates it from other physical vapor deposition methods already discussed. For a film to be grown by the CVD means, the precursor has to be delivered in the gas phase and transported to the substrate for the reaction to occur. The

CVD method has become an important thin-film deposition technology for a wide range of materials used in some areas of solid-state electronics requiring high purity of the material. In a CVD, the precursor is delivered in a gas stream and transported to the substrate with an application of energy leading to nucleation on the substrate.

A CVD technique is accomplished in different types depending on how the chemical reaction is initiated. A CVD reaction can occur under atmospheric pressure, low pressure or ultrahigh vacuum pressure. Several techniques are considered CVD based deposition methods, some of which are briefly outlined.

- Metal-Organic CVD (MOCVD): In the MOCVD growth method, metalorganic and other precursor chemicals are vaporized and transported as gases injected into the reactor at elevated temperature. This leads to a chemical reaction which results in the deposition of the crystalline film on the substrate [41]. The method can be used to create crystalline layers for multilayer structures and is a common method of film deposition in the optoelectronic industry.

- Plasma enhanced CVD (PECVD): In this method, a plasma is used to improve the rate of chemical reaction of the precursor. The PECVD growth enables growth at a lower temperature which is critical in the semiconductor industry.

- Aerosol assisted CVD - Also called mist-CVD, it relies on the precursors to be transported to the substrate by the means of liquid/gas aerosol generated through ultrasound pulses. This is a variant of the CVD method used for the growth of ZnO presented in this thesis. Further discussion of the mist-CVD growth method is presented in Chapter 4.

- Laser-induced CVD (LCVD): Still in its early stages of development, the LCVD uses a laser beam for a highly localized heating of the substrate that can then induce film deposition by the chemical reactions of the gases. Another mode of using the laser beam in the process is to activate gaseous reactant molecules/atom by absorption of light of a particular wavelength which can lead to a specific selection of atomic species for reaction and film growth.

2.4 Wet Chemical Methods

Film deposition through wet chemical routes typically involves the use of chemical bath and sol-gel methods where the precursors react to form colloidal solutions which form the basis of the growth species for the desired material. After allowing the precursor solution to age and evaporating the solvent, a continuous network of layers of the material is formed in a relatively simple manner. Films deposited using the wet chemical techniques are typically amorphous or un-oriented polycrystalline in nature with many grain boundaries resulting in low mobility and high resistivity, although post-growth annealing and plasma treatment can improve film properties [89]. A few of the reports on ZnO films deposited through the sol-gel methods are reported in these Refs [161, 63, 107]. The common wet chemical film deposition methods include

- Deep Coating: In this method, the substrate is dipped into a precursor solution and heated to vaporize the solvent thereby forming a continuous network of the solid film of the material. It is common for dip-coated films to be amorphous and requiring further annealing to achieve crystallization.

- Spin Coating: This method requires the precursor solution to be dropped onto an already spinning substrate enabling the precursor solution to spread across the surface forming a solid layer of film. Spin coating is employed in the course of my research for coating photoresist on the substrate for microelectronic device fabrication.

2.5 Basics of the Band Theory of Solids

Band theory describes the range of energies that an electron within a solid can occupy by looking at the quantum mechanical wave functions of an electron in the periodic lattice of atoms or molecules. From the band theory, the valence electron and the core electrons are localized. The core electrons, tightly bound to the nucleus do not interact strongly with adjacent atoms in a solid and have no net contribution to the bonding in solid. To describe the symmetry of the atomic orbitals in a crystalline solid, the wave vector k, has to satisfy the Bloch condition such that the allowed wave function must reflect the periodicity of the lattice [16]. These wave functions provide stationary solutions to the Schrödinger equation for an electron in a solid within the

periodic boundary conditions. For a free atom, the allowed energy levels are discrete in the form of atomic orbitals whereas, for solid, the energy levels for electrons form bands. The band theory provides a useful tool to understand several properties of solids including optical properties, electrical conduction, and magnetism.

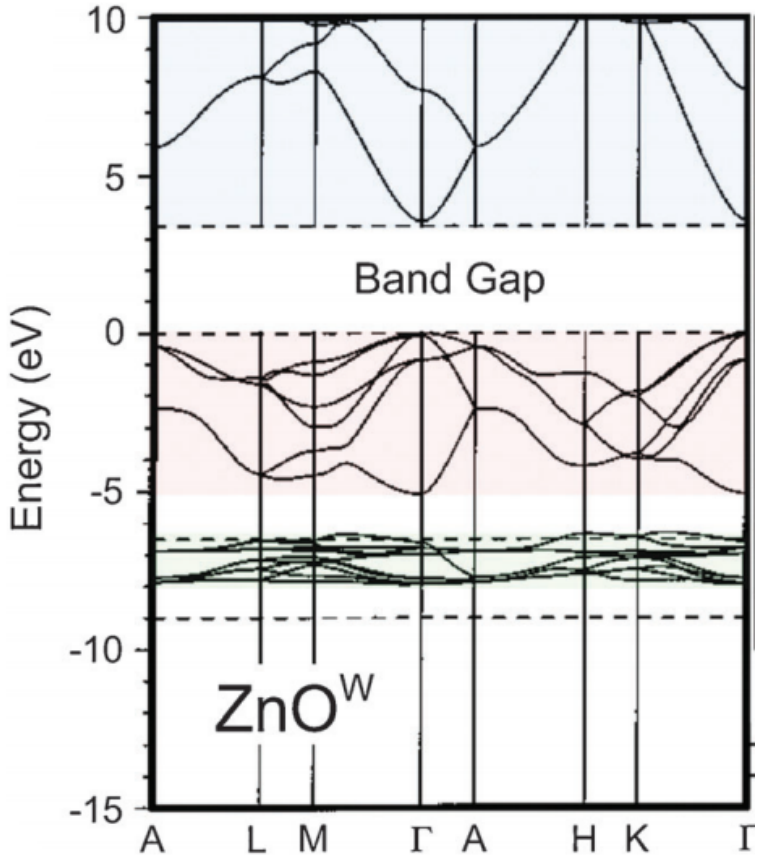


FIGURE 2.4: Electronic band structure of wurtzite ZnO calculated using local density approximations with self interaction correction (SIC-LDA) method [223].

It is typical for electrons to fill up lower energy bands first. The lower the energy band, the more likely it is filled by electrons. In a semiconductor, the top of the nearly filled band is the valence band while the lowest nearly empty band is the conduction band. A conductor, insulator or semiconductor can be understood in terms of the energy bands and their bandgap energy. The top of the valence and bottom of the conduction band are separated by the energy difference which is equal to the bandgap of the semiconductor. The band structures of a semiconductor and an insulator are similar except that insulators have a larger bandgap energy than semiconductors. Electrons in a filled band do not have net velocity, and hence do not conduct electricity. Conversely, an empty band does not contribute to current conduction.

It is understandable as to why the conduction band (via electrons) and the valence band (via holes) are the energy bands that contribute to current flow in solids.

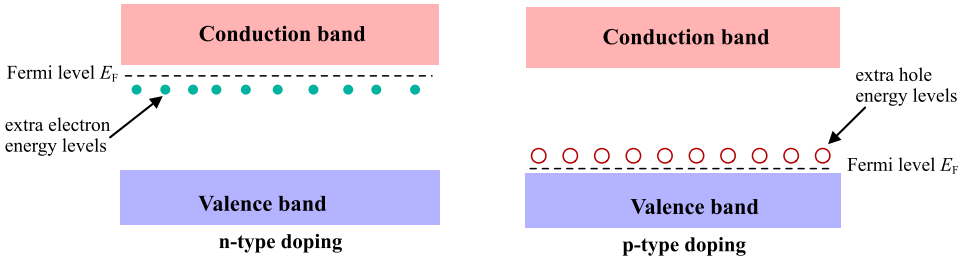


FIGURE 2.5: Representation of the position of the Fermi level E_F for a semiconductor with n-type and p-type conductivity.

The energy bands in solids are typically represented in dispersion graphs which are plots of energy versus the wave vector k. A band diagram depicting the electronic band structure of ZnO calculated using LDA model [223] is shown in Fig. 2.4. Whether the bandgap of a given semiconductor is direct or indirect is of fundamental importance in its applicability for optoelectronics. In a direct bandgap semiconductor, the energy difference between the valence band maximum and the conduction band minimum lies at the same k-point, usually the center of Brillouin zone (Γ-point) corresponding to k = 0 in the reciprocal lattice space. The difference in energy is the bandgap energy. In the process of optical or electron-phonon interactions, electrons can be excited with sufficient energy to move from the valence band to the conduction band [13, 50] resulting in the formation of holes in the valence band. In direct bandgap semiconductor such as ZnO, electron-hole pairs recombine radiatively with high probability.

An important quantity in the band theory is the Fermi level. At thermodynamic equilibrium, the Fermi level function is given as

$$f(E) = \frac{1}{1 + \exp(\frac{E - E_F}{k_B T})} \tag{2.1}$$

where $f(E)$ is the probability of an electron occupying a given energy state E at a particular temperature T, while E_F and k_B represent the Fermi level and the Boltzmann's constant respectively. The Fermi level is the energy level such that the probability that the energy state is occupied by electrons is exactly 1/2. At absolute zero, the value of the Fermi level E_F is called the Fermi energy and is constant for a given solid material. For semiconductors, the Fermi level lies within the bandgap which corresponds to energy state with a 50%

probability of occupation by electrons at a given temperature. The position of the Fermi level with respect to the conduction band determines the electrical properties of a semiconductor. The band theory gives an explanation of why metals are good electrical conductors due to their valence electrons being free, depicted as an overlap of the valence and conduction band such that a fraction of the valence electrons can move through the material and conduct electricity.

The addition of dopants to the crystal structure of a semiconductor can alter the position of the Fermi level. By doping with impurities that increase the net number of the electrons in the semiconductor material (n-type), the Fermi level moves closer to the top of the conduction band such that electrons can be easily excited to the conduction band as represented in Fig. 2.5. Similarly, if a semiconductor is doped with acceptor impurities thereby increasing the number of holes above the valence band, the Fermi level shifts down towards the top of the valence band. Further background knowledge on band structure and how explanations of material properties based on the theory can be found in a standard text on the Physics of semiconductors [210, 71].

2.6 Properties of ZnO

One of the reasons for the continued interest in ZnO arises from its desirable chemical and physical properties. ZnO has got piezoelectric properties and is also a wide bandgap semiconductor. It is transparent in the visible region and shows significant changes in conductivity when exposed to various chemical environments. These properties ensure that ZnO based semiconductors and other related materials remain potential candidates for applications in transparent conducting electronics, solar cells [194, 117], gas sensors [226, 193] and surface acoustic wave devices [82, 28] etc.

2.6.1 Crystal Structure

ZnO semiconductor typically crystallizes in the hexagonal wurtzite or cubic zinc-blende crystal structure similar to other groups II-VI binary semiconductors with each anion surrounded by four other cations at the corners of a tetrahedron and vice versa as shown in Fig. 2.6. At ambient conditions, the

wurtzite structure is stable and most common while the zinc blende structure can be obtained when the growth of ZnO is done on substrates with cubic lattice structure [173]. At relatively high pressure of about 10 GPa, ZnO undergoes a phase change to the rock-salt crystal structure.

The hexagonal wurtzite structure of ZnO has lattice constants: a = 3.252 Å and c = 5.213 Å, with a c/a ratio = 1.633 [173]. A schematic representation of the unit cell of wurtzite structure of ZnO crystal is shown in Fig. 2.6. A schematic diagram identifying the low-index crystal planes in hexagonal ZnO using the three-axis (Miller indices) and four-axis (Miller-Bravais indices) is shown. In the structure of ZnO, the Zn^{2+} ion is bonded tetrahedrally with an O^{2-} ions and vice-versa. The structure comprises of two interpenetrating hexagonal close-packed (hcp) sublattices, with each consisting of a type of atom displaced with respect to each other. Each sublattice has four atoms in each unit cell and every oxygen atom is surrounded by four zinc atoms and vice versa, which are coordinated tetrahedrally. Thus, the Zn terminated face (0001) and the O terminated face $(000\bar{1})$ constitute the polar faces while the $(11\bar{2}0)$ and the $(10\bar{1}0)$ faces which have equal O and Zn atoms constitute the non-polar faces. The polar nature of ZnO accounts for some of its interesting properties such as piezoelectricity, spontaneous polarization, crystal growth, and etching.

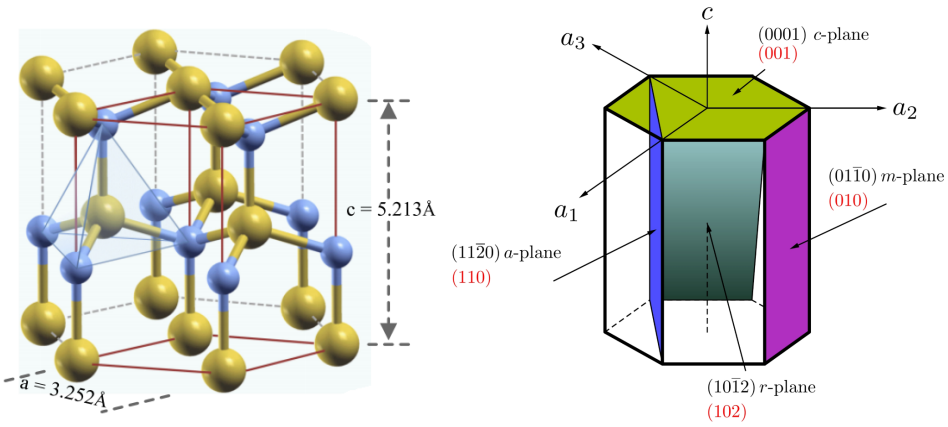


FIGURE 2.6: Hexagonal wurtzite crystal structure of ZnO. A sketch of the planes of a ZnO single crystal with their Miller indices indicated.

The tetrahedral coordination of ZnO is considered sp^3 covalent bonding although the electronegativity difference between Zn and O atoms gives significant bond polarity to ZnO. This makes ZnO substantially ionic with ionicity of 0.616 on the Philips scale [26], which is close to the borderline between covalent and ionic semiconductor. In addition to the piezoelectric property

of ZnO, the bond polarity in ZnO accounts for the preferential formation of hexagonal instead of the zinc blende crystal structure during growth [173]. The crystal structure and bonding in ZnO give it a mechanical advantage as a material with a high melting point of 1975°C, a beneficial property for the stability of electronic devices.

2.6.2 Band Structure and Optical Properties

Figure 2.7 is a schematic representation of the electronic band diagram of ZnO. As a direct bandgap semiconductor, the valence band maximum and the conduction band minimum occur at wave vector $k = 0$. Due to the effect of spin-orbit interactions and crystal field splitting, the valence band in ZnO is further split into 3 subbands named A, B, and C valence subbands. It is generally assumed in the academic literature that the symmetry of the A-valence subband is Γ_7 [85, 149, 19] even though it is debated based on the most recent magneto-optical studies in on free A-exciton and the free exciton oscillator strengths in ZnO [187, 68]. The middle subband (B-subband) and the C-subbands are known to possess Γ_9 and Γ_7 symmetries respectively [149]. The conduction band of ZnO originates from the empty 4s levels of Zn^{2+} in the ionic bonding or by the lowest anti-bonding sp^3 hybridization in the covalent scheme of bonding.

As a wide direct bandgap semiconductor, ZnO is a transparent material in the visible region of the spectrum with optical processes leading to emission and absorption are quite efficient since phonon interactions do not contribute to the interaction process. The band structure and the lattice dynamics of ZnO strongly determine the optical properties of ZnO.

The potential to utilize ZnO in optoelectronic devices is dependent on how efficient it emits or detects light which in turn is determined by the energy band structure and lattice dynamics. Excitation of a ZnO crystal of high quality with photon energy that is higher than the bandgap results in the transfer of electrons from the valence band to the conduction band. In the reverse process, electrons from the conduction band can return to the valence band to recombine with hole thereby emitting a photon with energy approximately equal to the bandgap of ZnO. The electrons and holes generated due to photon absorption can create an electron-hole pair. This coupled electron-hole pair held by Coulombic attraction is called a free exciton. Excitons in ZnO have binding energy as high as 60 meV, making it a material of choice for room temperature excitonic light emission and lasing. Excitons play an

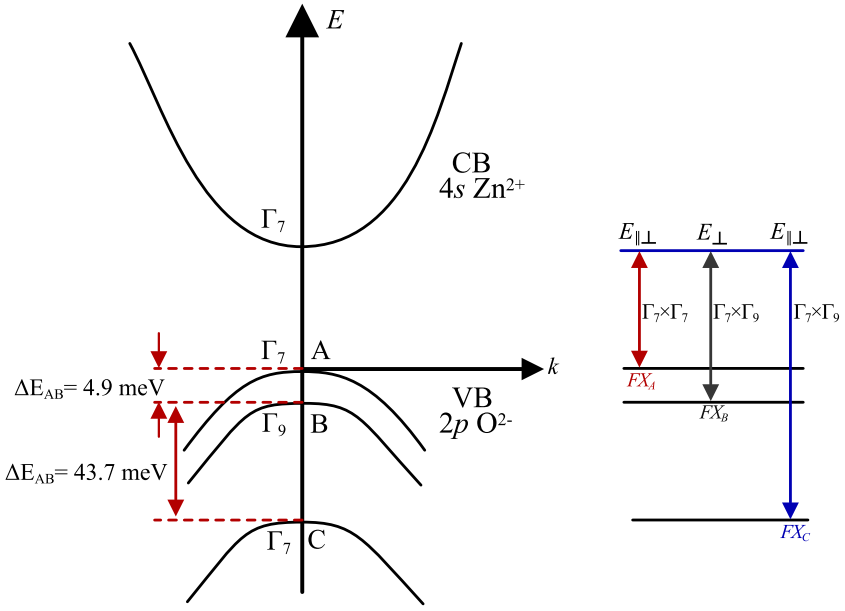


FIGURE 2.7: Representation of band structure of ZnO with with its intrinsic exciton ground state symmetries.

important role in the luminescence characteristics of ZnO. Optical transition studies in ZnO using photoluminescence spectroscopy and UV-Vis transmission/absorption spectroscopy are discussed in detail in Chapter 4.

2.6.3 Excitons in ZnO

The potential to utilize ZnO in opto-electronic devices is dependent on how efficient it emit or detect light which in turn is determined by the energy band structure and lattice dynamics. Excitation of ZnO crystal of high quality with photon energy that is higher than the bandgap results in the transfer of electrons from the valence band to the conduction band. The electrons and holes generated due to photon absorption create an electron-hole pair. This coupled electron-hole system held by Coulombic attraction is called a free exciton. An exciton can be considered analogous to the hydrogen atom with energy levels indexed by an integer n representing different energy states. These discrete energy states of excitons have binding energies expressed as [240]

$$E_{\mathrm{B,n}} = \frac{m_{\mathrm{r}}^{*} q^4}{2\hbar^2 \epsilon^2} \frac{1}{n^2} \tag{2.2}$$

where ϵ is the relative dielectric constant and m_r^* is the reduced mass of the exciton given by [123]

$$\frac{1}{m_{\mathrm{r}}^{*}} = \frac{1}{m_{\mathrm{e}}^{*}} + \frac{1}{m_{\mathrm{h}}^{*}} \tag{2.3}$$

m_e^* and m_h^* represent the effective masses of the electron and hole respectively. The exciton binding energy quantifies its stability against temperature. With an increase in temperature where thermal energy $k_B T$ is higher than the exciton binding energy, the exciton dissociates into an electron and hole. A recombination event and dissociation of an exciton results in an emission of characteristic photon that provides information about the energy and spatial position of the exciton [240]. Similar to the hydrogen atom, an exciton can be excited into higher energy levels represented with increased integer numbers n (i.e. n = 2,3,4,...). The formation of excitons in direct bandgap semiconductors due to photon absorption with energy $h\nu$ is given by [175]

$$h\nu = E_g - E_B(1/n^2) \tag{2.4}$$

where E_B is the binding energy of free exciton and E_g is the bandgap of the material. Conversely, excitons that recombine in an optical absorption process emit a narrow spectral line at photon energy given by Eq. 2.4. The binding energy of an exciton also depends on the dielectric constant of the material. Semiconductors such as Si and GaAs have high dielectric constant resulting in low exciton binding energy. Consequently, excitonic effects are only observed at low cryogenic temperatures in these materials.

As a result of possessing no net charge, excitons are not accelerated by electric field and cannot transport charge through the crystal [123]. Excitons can acquire kinetic energy given as [175]

$$E_{ke} = \frac{\hbar^2 k^2}{2(m_e^* + m_h^*)} \tag{2.5}$$

where k is the exciton wavevector associated with the motion of centre of gravity of exciton. The total energy of the exciton $E_{x,n}$ is written as [123]

$$E_{x,n} = E_g - \frac{E_B}{n^2} + E_{ke} \tag{2.6}$$

Due to the effects of spin-orbit and crystal field splitting in ZnO, the valence band of ZnO has three sub-bands, two with Γ_7 and the other with Γ_9. Group theory implies that the direct product of the band symmetries leads to intrinsic exciton ground state symmetries for the different transitions between the conduction band and the one of the valence sub-bands. The combination of these symmetries during transitions imposes a selection rule that is dependent on the polarization of incident electromagnetic waves. In relation

to A, B and C free sub-bands, the selection rule imposes that for polarized incident light with electric field $\boldsymbol{E}$ and wave vector $\boldsymbol{k}$ perpendicular to the crystal c-axis ($\boldsymbol{E} \perp \boldsymbol{c}; \boldsymbol{k} \perp \boldsymbol{c}$), transitions involving all the three excitons are allowed with the C-exciton weakly observable. If polarization is such that $\boldsymbol{E} \parallel \boldsymbol{c}$ and $\boldsymbol{k} \perp \boldsymbol{c}$, C-exciton is strongly allowed whereas the A-exciton is forbidden with the B-exciton only weakly observable.

In addition to the free excitons, excitons can be bound to shallow impurities and contribute significantly to the optical processes of the ZnO semiconductor at low temperature. A free exciton can bind to defects or impurities in the crystal structure to form bound excitons. A free exciton bound to a donor or acceptor forms a donor or acceptor bound exciton respectively. The energy positions and line width can be used to differentiate between a free and a bound exciton. The difference in the energy level between a free and bound exciton is equal to the binding energy of the bound exciton usually called the localization energy E_{loc}. The transitions involving bound excitons emit photons with energy given by

$$h\nu = E_{\text{g}} - E_{\text{B}} - E_{\text{loc}} \tag{2.7}$$

where E_{g} is the bandgap, and E_{B} and E_{loc} are the binding energy of the free and that of the bound excitons. Bound excitons are known for narrow spectral width and recombinations of bound excitons result in sharp line in a luminescence spectrum of ZnO at low temperature [175].

2.7 Defects and Doping in ZnO

To date, the various roles of impurities and defects in the electrical and optical properties of ZnO are not well understood. What is well known and reported is that as-grown ZnO material usually exhibits n-type conductivity. Since most of the growth of ZnO materials is usually done in a Zn rich environment, it was natural to assume that oxygen vacancies V_{O} and zinc interstitials Zn_{i} constitute the dominant donor defects and are responsible for n-type conductivity. However, the attribution of V_{O} and zinc interstitials Zn_{i} as the main source of conductivity had been challenged with theoretical calculations that showed both to have high formation energies in n-type ZnO and are deep rather than shallow donors [119]. Based on this argument, V_0 and Zn_{i} cannot be assigned as the predominant source of n-type conductivity. More so, their associated ionization energy will be too high to produce

free electrons. In contrast, some other theoretical analyses have concluded that Zn_i is actually a shallow rather than a deep donor [250, 165] and was experimentally supported through an electron irradiation experiment on bulk ZnO where Zn_i was identified as the shallow donor [137]. Despite this, the high formation energy associated with Zn_i still makes it a less likely source of n-type conductivity in ZnO. These theoretical calculations that attribute high formation energies for Zn_i and V_O in ZnO have led to a prevailing opinion that native defects do not contribute significantly to the conductivity in ZnO. However, this notion was strongly challenged with a view that native donors especially Zn_i contribute significantly to conductivity in ZnO, as complexes rather than isolated elements for which the theoretical calculations were based upon [137, 94].

Recently, the proposed origin for n-type conductivity in ZnO has now shifted to defects in the ZnO crystal resulting from H. With interstitial hydrogen serving as an amphoteric defect in most semiconductors [221], it has been reported that hydrogen exhibits shallow donor characteristics in ZnO and is easily ionized with a low formation energy which makes it abundant in ZnO crystal [228]. Experimental work on ZnO bulk material exposed to H during growth have confirmed that a shallow donor due to H contributes significantly to its conductivity [35, 205]. Apart from H, other donor impurities that contribute to ZnO conductivity include the Group III elements such as Al, Ga and In which easily substitute Zn atoms. Group VII elements such as F and Cl are also reported to act as donor atoms in ZnO [60] while Group IV elements such as C, Si, and Ge can be electrically active and act as donors or acceptors. Achieving p-type conductivity in ZnO with acceptor dopant atoms is of great interest in ZnO since it will lead to a p-n junction UV LED and could bring a similar impact in solid-state UV lighting that GaN made more economically. Group I elements such as Li, Na, and K, substituting for Zn, and Group V elements such as N, P and As substituting for O are considered as acceptors based on theoretical calculations [94]. Even though there are some reports of p-type conductivity achieved among researchers by incorporating these dopant atoms [139, 9, 153], a reproducible, reliable and stable ZnO of p-type conductivity remains difficult and challenging. Much of the problems stem from the low Hall mobility measured as well as localized carriers in ZnO films doped with these impurities thought to lead to p-type conductivity [173].

2.8 Thin film of ZnO

The application of ZnO in some areas such as optoelectronic devices, solar cells, gas sensing devices, thin-film transistors, etc, require material growth in the form of a thin film of thickness ranging from a few nanometres to microns. The texture of the film defines the orientation of the crystallites making up the film. The texture quality of the deposited film can be said to be in-plane or out of plane depending on whether rotation along the growth axis is the same for all the crystallites. A useful reference on the texture of ZnO films and a review of film properties for different deposition techniques is described in the cited thesis work [120].

It is rather expected that the physical properties and area of application of ZnO films can significantly be different from that of the single-crystal bulk material as determined by the microstructure and texture of the film. An instance is in the electrical performance of intrinsic and doped ZnO film where carrier mobility is determined by scattering within the grain and at the grain boundaries [53]. Therefore carrier mobility is decreased while electrical resistivity is expected to increase with decreasing grain size leading to more grain boundaries. Also, the performance of ZnO for use in acoustic wave devices is strongly determined by the maximum c-axis texture since the piezoelectric property of ZnO is only exhibited along that direction.

Further, the topography of the deposited ZnO film is another factor that is put into consideration in a technological application a thin layer of ZnO is used for. A smooth ZnO film topography is desirable, for instance when used as active channels for thin-film transistors. On the other hand, ZnO films with a crater-like rough topography will be suited for the front contact electrode in solar cell applications to effectively scatter the incoming light for better performance and efficiency [243].

Based on this premise, it is important to have a good understanding of the texture of deposited ZnO film and factors that control the growth to determine the application potential. It is also of interest to achieve thin film growth of ZnO with structural quality near a single crystal. An understanding of the mechanisms governing the growth of films is necessary to achieve nucleation tailored to a particular application. A discussion on the growth, texture and surface topography of mist-CVD deposited ZnO film is presented in a subsequent chapter.

2.9 Summary

A review of some of the thin film deposition techniques have been presented in the chapter. Generally, film deposition techniques can be grouped into methods involving physical vapor deposition or chemical vapor deposition techniques.

In the physical vapor deposition, the desired target material to be deposited is evaporated from the solid phase with the vapor condensed on the substrate. Vaporization of the target can be achieved via heating (thermal evaporation), high power laser (PLD), gaseous plasma (Sputtering) and via heating in effusion cell under ultra-high vacuum (MBE).

Chemical vapor depositions encompass methods that require chemical interactions to occur for film deposition to occur. Several methods of CVD based methods exist - MOCVD, PECVD, Mist-CVD are some examples.

Band theory of solids provides a theoretical model that describes the energy states of electrons in solid materials and provides a basis for the understanding of semiconductor characteristics such as optical and electrical properties.

ZnO is a direct wideband semiconductor with a hexagonal wurtzite crystal structure. It has an excitonic binding energy of about 60 meV.

Thin films of semiconductor material are required in certain applications as opposed to the bulk. Thin layers of materials could have physical properties that are different from that of the bulk.

Chapter 3

Film Deposition and Characterization Techniques

3.1 Introduction

This chapter is devoted to describe the experimental setup used for the mist-CVD deposition of ZnO films on substrates. It presents a discussion on the mist-CVD growth technique and focusses on the fine-channel mist-CVD design type for the growth of ZnO films. Some preparatory steps necessary for successful growth process are presented in addition to various characterization techniques used to study the film properties. The description of the basic principles behind these characterization methods are presented with results discussed in subsequent chapters.

3.2 Mist-CVD film deposition

In the previous chapter, a review of some thin film deposition methods was presented. Here, the discussion will focus on the mist-CVD growth technique for the deposition of thin layers of ZnO on various substrates. The mist-CVD is one variant of the conventional CVD growth process based on its underlying principle of a breakdown of precursor material by heat energy. The main feature of the mist-CVD growth technique is that it allows film deposition from source precursor in the liquid form delivered in the form of a mist. The mist is delivered to the heated reactor where evaporation of solvent occurs leading to chemical reaction and decomposition into a thin layer of desired material on a substrate. The system comprises two main units - the mist atomization unit and the reaction deposition unit. In the atomization unit, the source solution containing the constituent elements is atomized via an ultrasonic generator.

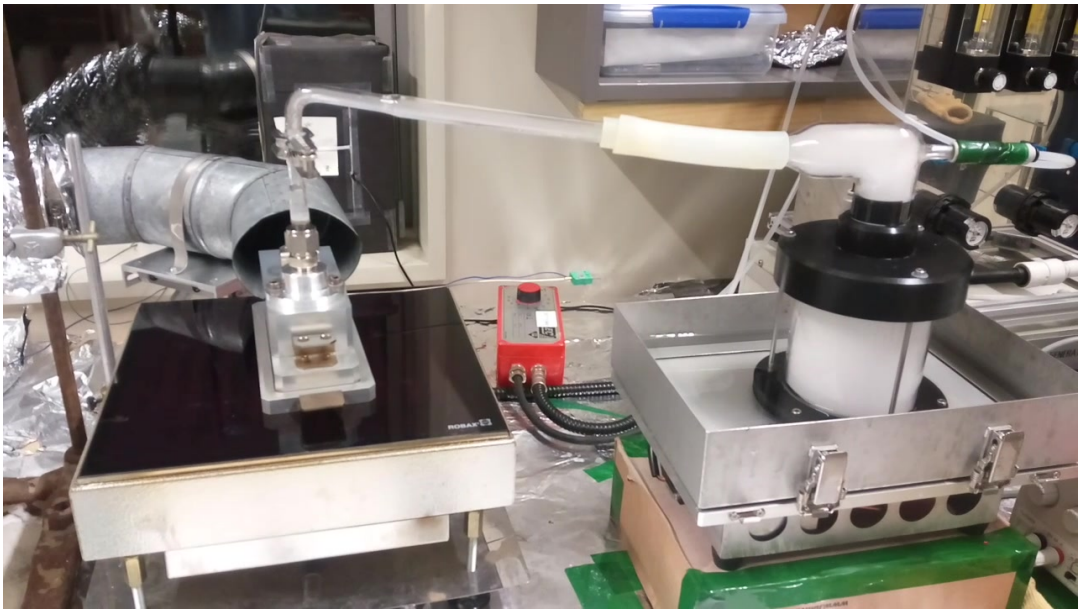


FIGURE 3.1: Photo of a mist-CVD system with a fine-channel reactor type used for the growth of ZnO films presented in this thesis. The reactor is insulated with refractory bricks during growth to maintain uniform temperature over the reactor.

As a solution-based growth method, the mist-CVD offers several advantages relative to other growth techniques. Mist-CVD is simple, relatively inexpensive and safe to operate. The technique allows for film growth under atmospheric conditions without any need for vacuum systems. Films can also be deposited on a large area substrate at relatively low deposition temperatures. The precursor salt used in mist-CVD is safe when compared with metal-organic salts used in MOCVD such as diethyl zinc and dimethyl zinc which reacts violently in air and water even at low-temperature [74]. Deposition of ZnO films throughout the research work used zinc acetate dihydrate $Zn(CH_3CO_2)_2.2H_2O$, widely used as the zinc source and is chemically stable in atmospheric air and cheap in cost.

The atomizing unit of the mist-CVD system consists of a container fitted underneath with three ultrasonic pulse transducers. Deionized water is usually poured into the container before placing the precursor chamber to prevent damage to the ultrasonic transducers. Each transducer is operated at a frequency of 2.4 MHz. The carrier gas is supplied from a pressurized oxygen gas cylinder. The flow of the carrier and dilution gases are controlled by a gas flow meter fitted with manual control knobs.

In the process of ultrasonic atomization, ultrasonic pulses are generated by the transducer which creates a fine mist of droplets that are ejected from

the precursor solution at very low velocity. The exact mechanism of atomization is still not well understood. There are two explanations for the mechanism of ultrasonic atomization of the liquid. One description is that ultrasound pulses induce vibrations into the liquid column which travel to the surface of the constituent liquid precursor and propagate as capillary waves. At a sufficient oscillation intensity that overcomes the surface tension forces of the liquid, the crest of these capillary waves extends into the droplets leading to atomization. The wavelength of the capillarity wave λ is given empirically as [140]

$$\lambda = \left[2\pi\sigma/\rho f^2\right]^{1/3} \tag{3.1}$$

where σ is the surface tension coefficient, ρ is the density of the liquid and f is the frequency of the surface waves.

Another hypothesis to explain atomization is the cavitation theory [215], which proposes that the disintegration of the liquid bubble and formation of micro-droplet mist is a result of vibrations from the ultrasonic pulses which cause regions of compression and expansion within the liquid column. A cavitation bubble is formed due to pressure wave propagating through the liquid. In the compression cycle, the positive pressure can lead to the implosion of the bubble to produce liquid droplet at the liquid surface. Presently, the most accepted theory combines the effect of both capillary wave and cavitation, with a hypothesis that the combination of capillary waves on the liquid surface in addition to cavitation bubble originating from acoustic oscillations beneath the liquid surface (i.e. cavitation) leads to the atomization of the liquid droplets [191]. Reported experimental observations have shown that the mean droplet diameter D is proportional to capillary wavelength on the liquid surface. At 2.4 MHz frequency, the droplet radius for atomized water is estimated to be 0.8 μm [104].

The mechanism that takes place in the growth of ZnO by the mist-CVD process remains debatable. Two models are considered to describe ZnO film growth in a mist-CVD deposition system. One of the mechanisms is the vaporization model as depicted in Fig. 3.2(a) which is similar to the gas source CVD where the constituent precursor is vaporized and film deposition occurs in the gas phase. The vaporization model is supported in the article by Lee *et al.* [131] and more recently by Uno *et al.* [219] who confirmed through secondary ion mass spectroscopy (SIMS) that the preferred growth mechanism for ZnO films in the mist-CVD system is the vaporization model. Another is the Leidenfrost model which describes film formation at the boundary between the droplet and the heated surface according to the Leidenfrost effect

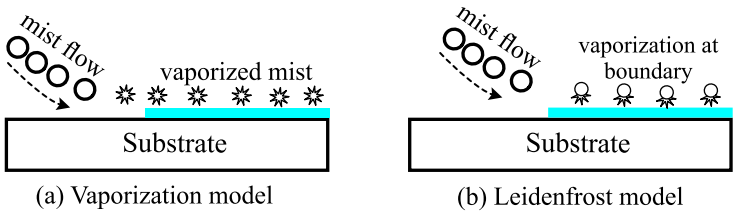


FIGURE 3.2: Depiction of two growth models in mist-CVD film growth: (a) Vaporization model and (b) Leidenfrost model.

[132]. The Leidenfrost effect is that rapid evaporation observed when water droplets touch a heated metallic pan or when liquid nitrogen is poured on a dry surface. This interaction enables the transfer of heat and mass between the mist droplet and the heated substrate until the complete evaporation of the droplet. In this model, the film deposition occurs at the boundary between the droplet and surface (Fig. 3.2b). Some articles have suggested the Leidenfrost effect as the mechanism for thin film deposition [103].

Most of the reports of film depositions using the mist-CVD system uses either of two reactor zone designs - (i) The fine-channel reactor (ii) The hot-wall reactor. The hot wall type is like the conventional MOCVD and can allow for high temperature growth and potentially high crystalline quality of films. For the hot wall design, it is expected that the atomized mist particles of the source material collide efficiently with the heated substrate. Depending on the design and other factors like mist flow rate and properties of the precursor solution, an efficient collision between the mist droplets and the heated substrate within the hot wall prevents complete vaporization of the precursor solution. Therefore, growth with the hot-wall system is more probable to follow the Leidenfrost process of film formation especially for solvent types such as water with a higher heat of vaporization compared with volatile alcohols. Nishinaka *et al* [163] used the hot-wall for ZnO film growth with a mixture of water and acetic acid (7:3 ratio) on a sapphire substrate with a buffer layer. Likewise, the work of Jonty Scott, a co-PhD candidate at the University of Canterbury has used the hot wall design type for the growth of SnO_2 films and other nanostructures.

All the ZnO films presented in this thesis were grown using the fine-channel mist-CVD reactor structure as described in the next section. Attempts made to grow ZnO film with the hot wall structure in the research work were achieved using only flammable methanol comprising $>$ 90% of the precursor volume. Such a precursor mixture was flammable and presented a fire safety risk, and in disagreement with the very desired merit of

the mist-CVD process as a safe film growth method.

3.2.1 Fine channel reactor

The reactor region where the deposition of the film occurs is made of aluminum and is of the fine-channel design structure. This reactor system initially developed by Kawaharamura, Kochi University Japan [103] schematically shown in the deposition stage of Fig. 3.3 consists of a thin "fine channel" region of about 1mm height above the substrate. The reaction region is narrowed to increase the film deposition efficiency by concentrating the vaporized mist gas on the substrate resulting in increased partial pressure for oxygen [105]. Thus, the use of the fine-channel mist-CVD reactor chamber supports film nucleation on the substrate via the vaporization model as reported by Lee et al. and Uno et al. [131, 219]. The fine-channel reactor was heated underneath through a heating plate with temperature monitored by a thermocouple attached close to the substrate in the fine-channel reactor. To maintain a uniform temperature within the aluminum-based fine channel reactor, refractory bricks were used to insulate the structure. Also, the refractory bricks allowed for good thermal insulation by preventing heat losses from convection and enabled stable temperature control over the entire fine-channel reactor. The relatively low melting point of aluminium ($\sim$660°C) constrained the deposition temperature for routine growth of films to 500°C with the fine-channel reactor. Even though a few depositions were done at a growth temperature of 550°C, degradation in the fine channel structure meant that growth temperature did not exceed 500°C for the majority of ZnO film samples.

During film growth using the fine channel reactor, the mist can be considered to move through four different stages.

- Evaporation: At this stage in the reactor, the mist particles carried by the transfer tubes move randomly and enter the heated cavity of the reactor. This is the stage that vaporization of the mist occurs. If multiple precursor reactants are transferred to the reactor, the mixing of the reactant species occurs in this zone.

- Vapour normalization: At this stage, the vaporized mist enters the fine channel reaction space. Due to the frictional interaction between the mist and the wall of the channel, the vapor moves with the laminar flow with uniform velocity.

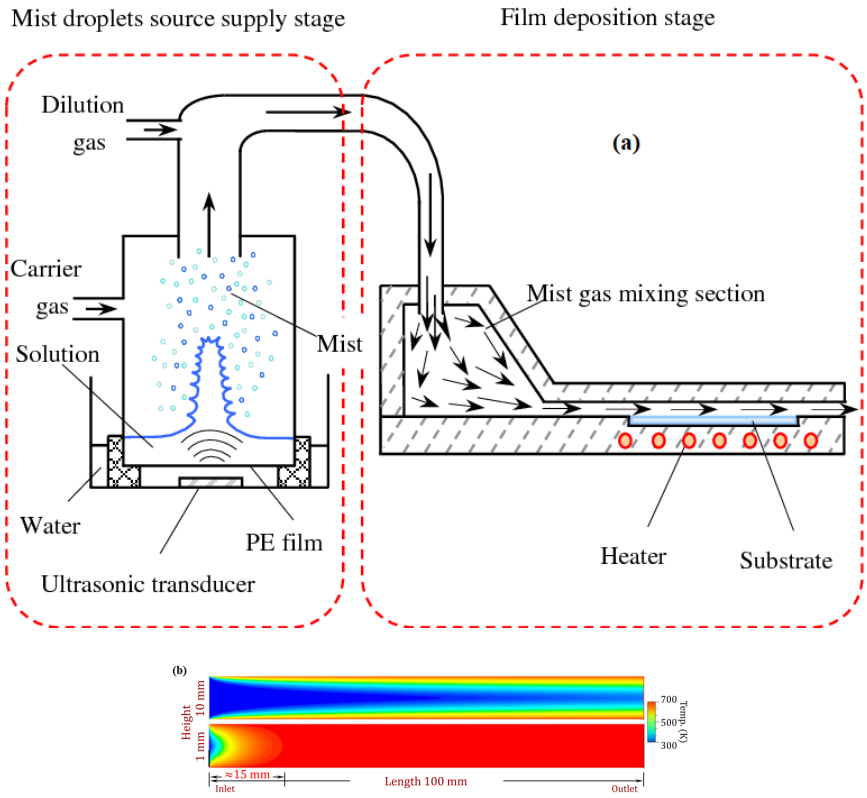


FIGURE 3.3: (a) A schematic diagram of the fine channel mist-CVD system with the ultrasonic atomization region and the fine channel structure with a reaction space of 1 mm height. (b) Temperature distribution based on numerical simulation for a 1 mm and 10 mm reaction space extracted from the work of [103].

- Deposition: The vaporized precursor growth species then reaches the substrate kept at a desired substrate temperature, and gains the needed activation energy resulting in film growth. By-products of gases and vapors are de-absorbed out of the surface of the substrate.

- Exhaust: This is the last stage in the reactor whereby vapors and gases produced from the film synthesis are moved outside of the reactor through an exhaust pump.

The very narrow channel in the FC-mist CVD provides a good thermal heat distribution across the reactor. The research article [103], provides an extensive work on the fine channel structure and shows through numerical simulation that temperature distribution in the reaction space that is 1 mm in height is significantly more uniform than a 10 mm reaction space as shown in Fig. 3.3(b). The temperature uniformity across the narrow reaction space

ensures that when a sufficient amount of precursor is supplied, the same reaction rate can be achieved in the whole reaction area. Such a feature allows for a uniform thin film growth across the entire substrate.

3.2.2 Pre-growth steps

Before the growth of ZnO film onto a substrate, various steps are taken including substrate cleaning and precursor preparation. These steps are routinely taken whenever ZnO film is grown. Most of the film depositions were done on a 10 mm $\times$ 10 mm substrate area. That area is usually diced from a 2-inch diameter sapphire wafer. First, the 2-inch wafer is carefully mounted on a silicon wafer 4-inches in diameter to provide a base for the sapphire and to prevent damage to the sapphire wafer. The sapphire wafer is spin-coated with AZ1518 photoresist to protect the polished surface from debris that occurs during dicing. A wafer saw is used to cut deep into the sapphire wafer without going right through the wafer thickness to the desired area (typically 10 mm $\times$ 10 mm).

Both the sapphire substrate and ZnO film being transparent presents a challenge in identifying the correct side of the substrate that has film deposited on it. The identification of the film surface is done by making an inscription mark using a diamond scriber on the opposite substrate surface where film deposition was not done.

Substrate cleaning

The cleaning of the substrate is vital in the film deposition process with contamination of the substrate surface able to cause nucleation sites facilitating growth and leading to non-uniform film deposition. For each film growth procedure, the substrate cleaning process typically comprises of ultrasonic agitation for 10 minutes each in acetone, methanol and isopropyl alcohol (IPA). After cleaning in IPA, the substrate is blow-dried using nitrogen gas.

Since a layer of photoresist is used to protect the surface of the substrate during dicing to desired sizes, a further cleaning step using oxygen plasma is done before the growth of films to remove residual particles of photoresists that may not have been removed by ultrasonic agitation in the cleaning process.

Precursor Solution

For film deposition, the precursor solution consists of a mixture of zinc acetate dehydrate dissolved in aqueous ammonia solution. The ammonia solution is maintained at the desired pH by measuring it with a calibrated digital pH meter before the addition of zinc acetate salt. The solution is magnetically stirred at room temperature for about 20 - 30 minutes to ensure that the zinc acetate salt is completely dissolved and a clear solution is formed.

A completely clear precursor solution is then transferred to the atomization chamber where ultrasonic pulses from the transducer enable mist to be generated from the solution. Before the growth of the ZnO film, a warm-up process of 5 minutes duration is done by atomizing the precursor solution without any flow gas. A carrier and dilution gas flow rates of 4 lit/min and 6 lit/min were respectively set to transfer the generated mist particles to the heated reactor. For each growth, source precursor volume of about 150 ml is transferred into the atomization chamber and replenished after 60 minutes of growth if necessary.

3.3 Characterization Techniques

In this section, the various characterization techniques that were utilized to study the properties of ZnO films deposited through the mist-CVD growth process are described. These characterization techniques were used to study the morphological, electrical and optical properties of the films. The crystalline properties were investigated through X-ray diffraction measurements.

3.3.1 Film Surface Morphology

Surface morphology of deposited films was studied using atomic force microscopy. An understanding of film morphology and the factors that influence morphology are useful considerations in optoelectronic applications, with rough film surfaces contributing to electron scattering which affect the performance of metal contacts when films are employed in electronic devices. A smooth surface morphology of a film sample entails an increased likelihood of fewer grain boundaries and better electrical conductivity within the bulk. Also, since thin films are grown on substrates, the surface tension at

film-substrate interface and wetting/de-wetting processes in the film crystallization play vital roles in determining the film morphology [136]. Additionally, factors such as temperature, vapour atmosphere, precursor concentration and surface treatment affect and lead to different film morphologies. The description of two methods utilized for surface morphology studies of deposited films is discussed.

Atomic force microscopy

Atomic force microscopy (AFM) is used to acquire high-resolution images of the sample surface using the atomic force interactions between the sample surface and the scanning tip. In the AFM, the tip which is fixed to the cantilever interacts with the surface of the sample resulting in the deflection of the cantilever beam in line with Hooke's law. At a very close distance between the tip and the sample surface, the attractive and repulsive forces between the tip and the atoms of the sample act as a net force on the probe tip and deflect the cantilever. Thus, the net force between the probe tip and the sample surface is proportional to the displacement of the cantilever. While the probe tip scans across the surface of the sample, a photo detector measures a laser beam that reflects off the cantilever. The laser monitors the net deflection of the cantilever enabling a topographic image of the sample surface to be constructed.

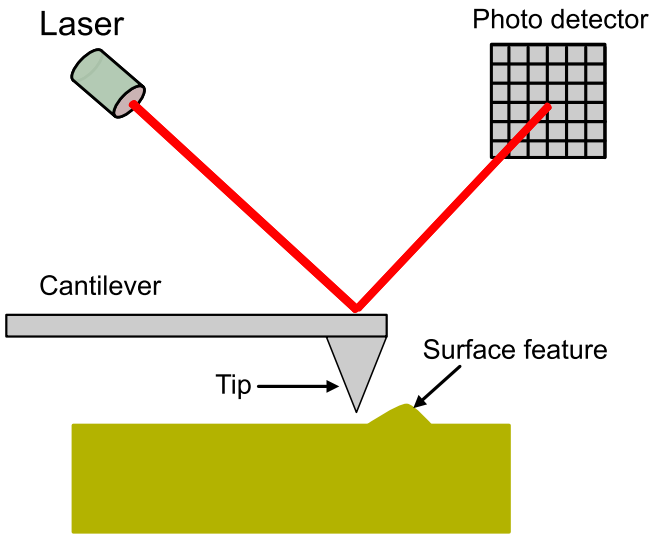


FIGURE 3.4: Schematic representation of the working principle of atomic force microscope (AFM)

There are commonly two modes of measurement utilized for surface imaging in the AFM - (i) contact mode which requires that the scanning tip is in contact with the surface (b) tapping mode where the molecule orbitals of the cantilever tip and the surface overlap and interact through electrostatic forces. The AFM images presented in this thesis were all acquired using the tapping mode to reduce the possibilities of damage to the film surface and the tip. Analysis of AFM images was done with Gwyddion software. An important assessment of film morphology using the AFM is the root-mean-square roughness (R_{rms}) based on the relation [186],

$$R_{\text{rms}} = \left(\frac{\sum_{i=1}^{N} (Z_i - Z_{\text{avg}})^2}{N} \right)^{1/2} \tag{3.2}$$

where N is the number of points, Z_i is the ith point of Z and Z_{avg} is the average value of Z.

3.3.2 Optical Characterization

Two characterization techniques were employed to study the optical properties of the ZnO films deposited by the mist-CVD process. These methods are the UV-Vis absorption/transmission spectroscopy and photoluminescence (PL) spectroscopy.

UV-Vis spectrophotometry

For the transmission and absorption spectroscopy of ZnO films, a Cary 6000i UV-Vis-NIR spectrophotometer capable of recording spectra from the UV to near infrared region was employed. The spectrophotometer comes with 2 sets of lamps - one is a hydrogen lamp that is best suited for measurement in the UV region between 200 - 350 nm while the other is a quartz-iodide lamp that is optimized from ultraviolet to the near infra-red region between 300 - 1800 nm wavelength.

During transmission measurement, a light beam of varying wavelength from 200 nm - 800 nm is selected through a monochromator (with a default spectral bandwidth of 2 nm) and split into two beams - the sample and reference beams. To compensate for the varying intensity of light source at different wavelengths, an absolute value of transmission spectra was not recorded.

Instead, transmission signal from a sample with film deposited on it is compared to a reference beam passing though a bare substrate. This enables effects from the reflectivity constants of the substrate to cancel out and allows transmission measurement only from the film to be recorded. Additionally, a baseline calibration is done to correspond with 100% and 0% through the sample. Such calibration is necessary to remove the discontinuities in the spectrum that may show up during lamp changeover.

Measuring the transmission/absorption of photons of varying wavelength through a semiconductor provides a direct method to find the optical properties of the material such as bandgap and absorption coefficient $\alpha(\lambda)$. The electronic state of a semiconductor material is shown in its optical absorption properties thus, information related to these electronic states can be found from transmission spectroscopy.

The Beer Lambert law written as $I = I_0 \exp(-\alpha d)$ gives the intensity of transmitted light incident on a material with thickness d and absorption coefficient α. The percentage transmission and absorption coefficient α are expressed using the following equations

$$\%T = \left(\frac{I_t}{I_0}\right) \times 100 \tag{3.3}$$

$$\alpha = \frac{1}{d} \ln \left(\frac{I_0}{I_t}\right) \tag{3.4}$$

$$\alpha = 2.303 \frac{A}{d} \tag{3.5}$$

where I_0 is the light intensity transmitted along the reference beam and I_t is the intensity transmitted from sample.

The absorption spectra are calculated from the measured transmission through the film sample. The absorbance A is calculated from transmission using the relations

$$A = 2 - \log \frac{\%T}{(1-R)^2} \tag{3.6}$$

where A is the absorbance, $\%T$ is the transmission through the film in percentage and R is the reflectivity. In this thesis work, the reflectance is not taken simultaneously with transmission data because the reflectance is almost constant in the visible region. The transmission spectra for the deposited films shows close to 100% transmittance in the visible spectrum.

Therefore, the reflectance is ignored and the absorbance is simplified as $A = 2 - \log(\%T)$.

In the high absorption region, the variation of the absorption coefficient is used to determine the optical band gap and obey the Tauc relation [213],

$$\alpha h\nu = B(h\nu - E_g)^n \tag{3.7}$$

where E_g is the optical band gap and B is a parameter that is independent of the photon energy. The value ascribed to n depends on the type of electronic transition taking place during photon absorption. In crystalline semiconductors and assuming a parabolic density of states, n can take the value of $1/2$, 2, $3/2$ or 3 depending on whether the transition is allowed direct, allowed indirect, forbidden direct or forbidden indirect respectively. With ZnO being a direct bandgap semiconductor, the allowed transition dominates the basic absorption process with $n = 1/2$ used the determine the optical bandgap. Since the absorption coefficient, α is defined as absorbance A divided by the film thickness, the extrapolation of the linear region in the plot of $(Ah\nu)^2$ against photon energy estimates the optical bandgap.

Photoluminescence Spectroscopy

A lot of interest in ZnO focusses on its optical and luminescence properties. The photoluminescence (PL) spectroscopy technique is a non-destructive process to study the electronic band structure and allows optical and defect features to be identified based on the emission lines observed on the spectra. PL studies can also give additional information on the crystal quality of a material that is investigated. For ZnO to be effectively utilized in optoelectronic applications, a good understanding and characterization of its optical emission are necessary.

In a semiconductor, photo-excitation of the material occurs when photons with energy greater than the bandgap interact with the semiconductor material. The result of photo-excitation is that electrons are promoted from the valence band to the conduction band with a hole left behind by the excited electron. The electron eventually transitions back to equilibrium ground state. The photons emitted in a PL spectrum arise due to electronic transitions and hence, provides information on the electronic energy levels of the material. In a direct bandgap semiconductor such as ZnO, a more probable outcome is the emission of photons with energy approximately corresponding to the bandgap energy of the semiconductor. The excitation of electrons to the con-

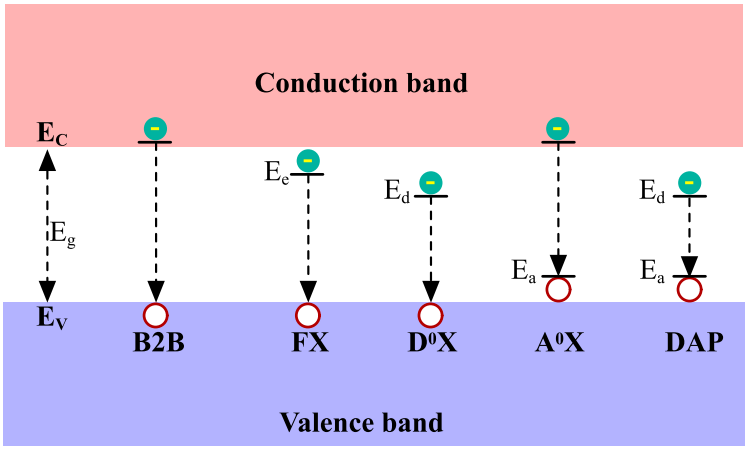


FIGURE 3.5: Representation of different radiation recombinations in a semiconductor - (B2B) Band to band, (FX) free exciton, (D^0X) donor bound exciton, (A^0X) acceptor bound exciton and (DAP) donor-acceptor pair.

duction band by the external source leads to several recombinations mechanisms as illustrated in Fig. 3.5. A band-to-band (B2B) recombination occurs when a free electron in the conduction band recombines with a hole in the valence band. This type of transition dominates at room temperature resulting in a broad peak at the bandgap energy of the material. At low cryogenic temperature, exciton formation probability increases leading to the observation of emission with excitonic origins. Emission can be from a free exciton and can be bound to native defects, impurities and crystal imperfections. Bound excitons are localized and trapped to the defect sites formed by impurities in the crystal. These impurities can be a donor or acceptor resulting in donor bound D^0X or acceptor bound A^0X excitonic emissions respectively. As a result of energy used for bonding, bound excitonic emission has photon energy that is red-shifted compared to that of the free exciton. By detecting the PL features associated with these defects during radiation recombinations, impurities in the crystal can be identified. ZnO being an intrinsic n-type semiconductor, there is a relatively high concentration of donors within the crystal, hence the presence of excitonic recombination from a neutral donor is commonly observed in ZnO at low temperatures. The Coulomb attraction between an electron and the hole forms a coupled quasiparticle electron-hole system called exciton [93, 115]. An exciton can be free to move within the lattice and can have an effective radius of multiples of lattice constants. Such is referred to as free exciton (FX), or Wannier-Mott exciton and is observed in most semiconductors. An exciton confined to its excitation site is called a Frenkel exciton mostly found in an insulator and molecular crystals. For an

intrinsic ZnO crystal, PL emission is dominated by excitonic recombinations and their longitudinal optical (LO) phonon-assisted transitions.

A schematic representation of the PL measurement apparatus is shown in Fig. 3.6. The excitation laser source is a 25 mW He-Cd laser with a wavelength emission at 325 nm (3.815 eV) which enabled excitation of the ZnO samples above the bandgap energy. The ZnO samples are affixed on a copper finger sample holder using a silver paste and contained within the cryostat. For temperature-dependent PL measurement, heating of the sample is provided by Oxford Instrument Intelligent Temperature Controller. The inci-

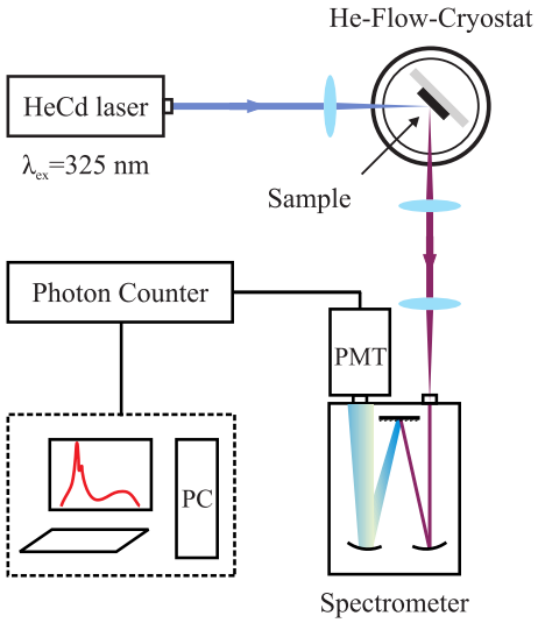


FIGURE 3.6: Experimental setup for the acquisition of PL spectrum from ZnO film sample.

dent laser beam angle was maintained at 40 - 60° to the normal of the sample surface which allowed for discrimination of reflected light from the actual photoluminescence originating from the sample. PL emissions that are perpendicular to the sample are collected and collimated by a short focal lens and then focussed on to an SP2150 spectrometer by a longer focal length lens. All lenses used in the experiments have high transmission in the UV region (> 92% @ 365 nm). The PL intensity spectrum spanning from the ultraviolet to the near infra-red regions is collected and stored on a computer.

3.3.3 Point probe Hall effect

Hall effect electrical characterization is used to measure the charge carrier concentration, type of charge carrier, mobility, and resistivity of a material.

The underlying basic principle of the Hall effect is illustrated in Fig. 3.7. When a constant current I flowing through the sample encounters a uniform magnetic field with strength B perpendicular to the direction of current, the current charge carrier q drifting with a velocity v will experience a Lorentz force given by $F_B = qv \times B$ perpendicular to both the direction of current and magnetic field. The result as illustrated in Fig. 3.7 is that the charge carrier is deflected in the y-direction. In an n-type semiconductor material such as ZnO with current I passing through a sample, the electrons reach a steady state with drift velocity given by

$$v = \frac{I}{nAq} \tag{3.8}$$

where n is the charge density, A is the cross-sectional area and q is the electron charge. When an externally applied magnetic field B is in the direction perpendicular to the current flow, electrons will accumulate at one edge of the sample. The force experienced by the electrons is given as

$$F_B = \frac{IB}{nA} \tag{3.9}$$

These accumulated electrons create an electric field E_H due to the uneven

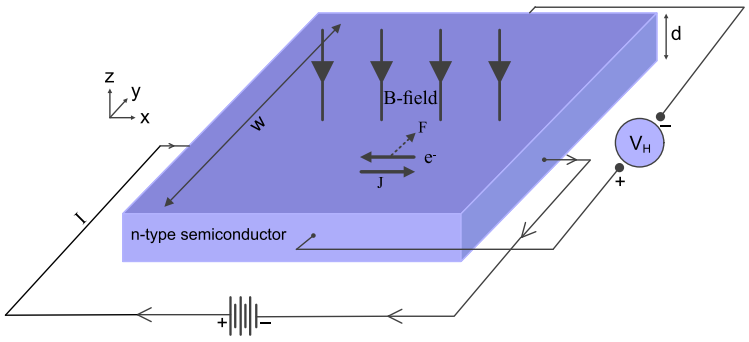


FIGURE 3.7: Schematic representation of the principle of Hall-effect leading to a Hall voltage V_H.

distribution of charges with a measurable potential difference known as the Hall voltage V_H. The current continues to flow along the material which indicates that the force on the electrons due to the Hall electric field E_H balances that of the magnetic force. Hence,

$$E_H = \frac{IB}{qnA} \tag{3.10}$$

The magnitude of the Hall voltage V_H is the E_H multiplied by the width of the material w. Since the sheet density n_s is defined as the density of electrons multiplied by the thickness of the material, V_H can be defined in terms of n_s as

$$V_H = \frac{IB}{qn_s} \tag{3.11}$$

For a sample of roughly square geometry, the van der Pauw method configuration method is widely used to determine the electrical properties of the sample. The van der Pauw geometry entails four electrical contacts at the four corners of the square sample. This measurement geometry is also applicable to other arbitrary shaped samples as long as the sample thickness is defined and uniform, the contact area is small and are all on the perimeter of the sample. In the work presented in this thesis, a HEM-2000 Hall Effect System from EGK Holdings with a 0.51 T magnet was used to perform Hall effect measurements on samples 5 mm $\times$ 5 mm utilizing the Van der Pauw geometry. The Van der Pauw method involves measuring the resistivity of a sample material through a 4-point probe contact method by applying current at one edge of the sample and measuring the voltage across the opposite edge. The sheet resistance of the sample can now be determined by solving the Van der Pauw formula given by [180]

$$\exp\left(\frac{-\pi R_{\text{vert}}}{R_s}\right) + \exp\left(\frac{-\pi R_{\text{horiz}}}{R_s}\right) = 1 \tag{3.12}$$

where R_s is the sheet resistance (Ω/sq) and, $R_{\text{vert}}$and R_{horiz} are the averaged resistances measured in the vertical and horizontal edges of the sample. For a known thickness of sample d, the resistivity ρ is found by the relation,

$$\rho = R_s d \tag{3.13}$$

The mobility of majority charge carrier called Hall mobility μ_H can be calculated from the sheet resistance and carrier density using [211]

$$\mu_H = \frac{1}{qn_s R_s} \tag{3.14}$$

It can be noted that the above derivations apply to the condition of sample homogeneity with only a single type charge carrier responsible for current transport. This condition is most times not usually met in materials such

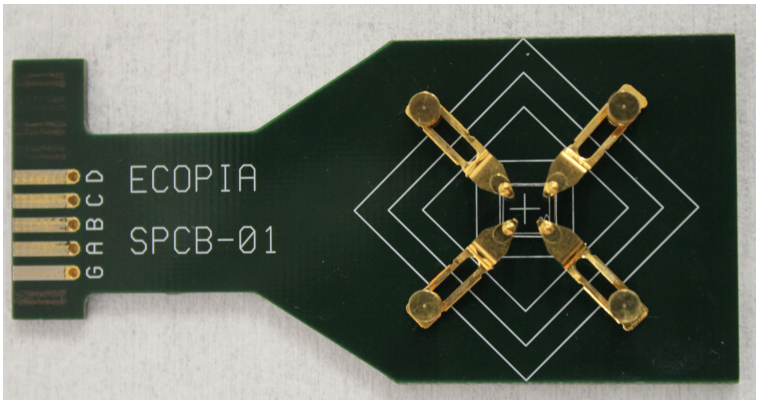


FIGURE 3.8: A Hall effect board with a mounted 5mm × 5 mm ZnO film sample for electrical measurement.

as ZnO. There can be parallel conduction paths within the sample with different mobility or charge carrier concentration. Additionally, surface states are well known to occur in ZnO stemming from polarity related near-surface band bending and adsorption of ambient gases [3]. Typically, to investigate mixed conduction mechanisms in a sample, temperature-dependent Hall effect measurement is done and fitted with a two-layer model to determine the mobility of individual charge carriers [138]. The results from the Hall effect measurements reported in this thesis were done at room temperature which gives effective mobility of the majority charge carrier.

3.3.4 X-ray Diffraction

When electromagnetic radiation impinges on a structure that is periodic with geometric length variation on the scale of incident wavelength of radiation, diffraction effects are observed. The interatomic distance in crystalline solids is about 0.15 - 0.4 nm, corresponding to the x-rays with photon energies between 3 and 8 keV. Therefore, exposing a crystalline solid to x-rays enables observable effects such as constructive and destructive interference, which are exploited to study structural properties like lattice parameters, strain and epitaxial quality.

A diffracted beam can be observed when certain geometric conditions are satisfied. If the distance between two adjacent crystal planes, given by the inter-planar spacing d_{hkl} and the x-ray beam incident at an angle θ differ by an integer number of wavelengths, constructive interference occurs leading to a diffracted beam emitted at an angle of 2θ. This condition for an efficient diffraction pattern from crystal planes identified by their Miller indices is

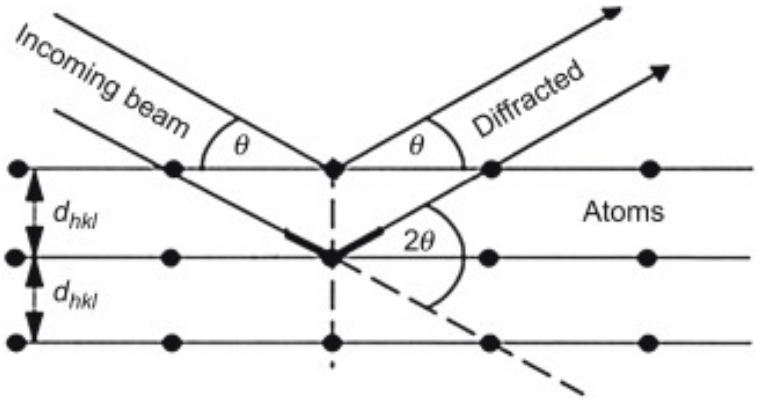


FIGURE 3.9: Visualization of diffraction from planes in a solid crystal. The intensity of the diffracted beam is maximum at Bragg's condition.

known as the Bragg's law.

$$n\lambda = 2d_{\text{hkl}} \sin\theta \tag{3.15}$$

where n is an integer and d_{hkl} is the inter-planer spacing in the lattice while θ is the diffraction angle measured as an angle between the incident beam and the crystal plane as represented in Fig. 3.9.

Typically, the wavelength of the x-ray is fixed, determined by the source of the x-ray. The diffraction pattern formed by a specific set of planes in the crystal with d_{hkl} spacing produce diffraction peaks. The peak position in the XRD spectra is determined by the inter-planar atomic spacing which obeys the Bragg's diffraction law and the atomic planes are identified with Miller indices.

X-ray diffraction experiments were performed with a Rigaku Powder X-ray Diffractometer (PXRD) equipped with a Bruker CCD area detector specifically designed for powder XRD measurements. The diffractometer comprises of a copper target x-ray source which produces a K-α radiation at a wavelength of 1.5406 Å. Additionally, a stepping motor assembly called goniometer enables both rotation and translation of the sample and detector during sample alignment and measurement. As is common with PXRD systems, diffraction analyses are performed with the Bragg-Brentano geometry. This measurement geometry is quite different from grazing incidence XRD (GIXRD) noted to be more suitable for thin film samples. A brief explanations of Bragg-Brentano geometry is presented here with some contrasting features between its configuration and that of GIXRD.

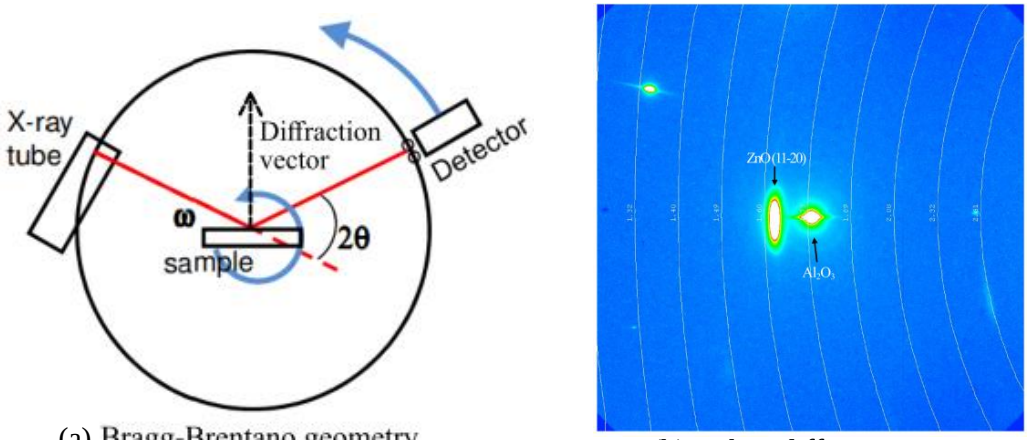
Bragg-Brentano geometry

This geometry is commonly used with for XRD analyses of powder samples. A typical equipment design that is considered as Bragg-Brentano configuration used parafocussed x-ray source that is fixed while the sample is rotated around θ and the detector moves by 2θ. Additionally, a vector called the diffraction vector that bisects the angle between the incident and scattered beam is always normal to the surface of the sample during measurement. The parafocussed x-ray source in this geometry is not really focussed but is a divergent beam from a sealed tube, thus avoiding reduced intensity linked to focussed and parallel beams [45].

In a diffraction measurement, x-rays from the source are scattered in a sphere around the sample while the detector moves in a circle around the sample with the position of the detector assigned to the angle 2θ. The number of x-rays observed at each angle of 2θ is recorded by the detector as counts. The randomly oriented crystallites in the sample produce Debye diffraction cones (in the sphere) that correspond to a single Bragg angle 2θ. The linear diffraction pattern is obtained when the detector scans through an arc that intersects each Debye cone at a single point. The diffraction pattern of a crystal which consists of positions, integral intensity and line profile of diffraction effects obtained as a digital image are called Debye rings as shown in Fig. 3.10(b). Post-processing of the the Debye ring images enables a plot of intensity vs. 2θ angles to be obtained.

In the ω scan, a 2θ angle is kept constant while the angle ω is varied. Since the contribution in the diffracted beam ideally comes from regions within the sample with well-defined lattice spacing, varying ω allows tilts in the crystalline arrangements for a given lattice plane. The ω scan is referred to as the "rocking curve" with the Full-Width Half-Maximum (FWHM) of its peak used to evaluate the structural quality of epitaxial layers.

It is important to note here that unlike the grazing angle incidence configuration (GIXRD), characterization of thin films using the Bragg-Brentano geometery generally produces weak signals from the film with intense peak from the substrate [18]. Additionally, the parafocussing optics used in the Bragg-Brentano configuration causes the width of diffraction peaks to become larger as a result of defocussing effects since the exposed area on the sample surface is wider when tilted [160]. Other drawbacks associated with the parafocussing Bragg-Brentano geometry include the requirement for very precise alignment, with even slight errors leading to difficulties in determining crystal orientation. In fact, the Bragg-Brentano is suited for powder



(a) Bragg-Brentano geometry

(b) Debye diffraction ring

FIGURE 3.10: (a) Schematic of x-ray powder diffraction system with the Bragg-Brentano measurement configuration (b) Typical Debye diffraction ring image obtained for ZnO film sample.

diffraction where it is expected that different orientations of crystallite in the sample contribute to diffraction pattern.

A GIXRD configuration for thin films uses collimating optics to produce an intense parallel beam. For diffraction measurement, a small incident beam angle (typically between $1 - 5^{\circ}$) is fixed while the angle between the incidence beam and the diffracted beam (2θ) is varied. The small incidence angle results in the path travelled by the x-ray to increase on the film surface thereby reinforcing the diffraction pattern from the film while suppressing effects from substrate. Also, in contrast to the Bragg-Brentano configuration which probes only lattice planes aligned parallel to the surface, GIXRD probes grains in all directions.

Post processing of the Debye ring diffractrograms was performed to extract diffraction angle and rocking curve information. A software called CrysAlisPro was used for data analyses. Plots of intensity vs 2θ were generated by integration of pixel values in the Debye ring image along the 2θ diffractions angles. The rocking curve analyses for a given diffraction peak angle 2θ are obtained from the Debye ring image by binning and integrating pixels enclosed by a thin mask centred at the peak in the azimuthal direction.

3.4 Film thickness

The thickness of deposited film plays a major role in determining its properties. For microelectronic applications, film thickness needs to be precisely controlled and reproducible. Some methods were used to determine the thickness of the film samples presented in this thesis. The main methods include the use of profilometer, profiling with the AFM, and thickness measurement from optical interference extrema.

Profilometer

The stylus profilometer enables the thickness of the film sample to be found. By etching off the film on an area of the film, a well-defined step edge produced from the etching process enables a direct thickness determination using the stylus profilometer such as one shown in Fig. 3.11. The profilometer works by producing a vertical translation of the stylus due to surface variation when the stylus tip moves across a film surface. Thus, the etched region of the film provides a step edge that enables accurate determination of the film thickness.

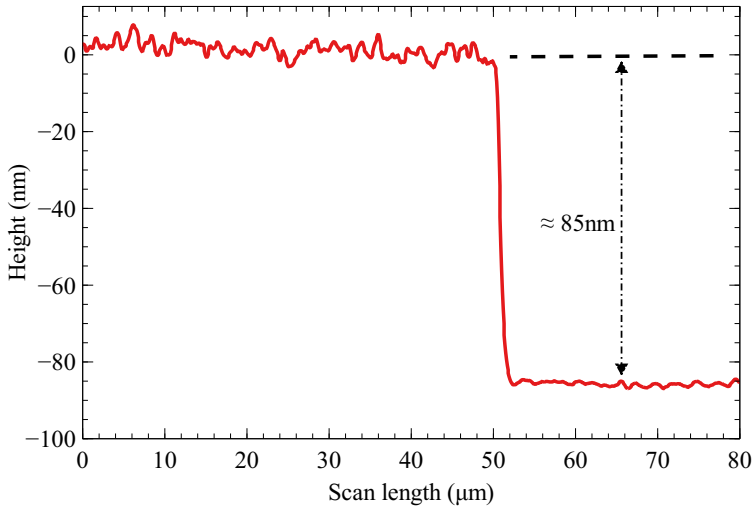


FIGURE 3.11: Graph showing a profilometer scan across the stepped edge formed from etching process on ZnO film. The film thickness was found to be 85 nm.

The deposited film sample is initially prepared for thickness determination by spin-coating the film with a photoresist (MicroChemical GmbH AZ 1518) and soft baking it at 96°C for about 5 minutes to ensure that the photoresist is dry and adheres to the film surface. As a positive photoresist, the AZ 1518 becomes soluble in a chemical developer after being exposed to UV

light. To selectively expose an area of the film to UV light, a quick photolithographic step was done with a photomask which effectively creates an area on the film that is exposed to UV light and other areas masked from UV. After UV exposure, immersion of the film in a chemical developer led to region on the photoresist coating exposed to the UV light to become soluble thus, exposing the underlying film. The film sample is then rinsed with deionized water thereby leaving some film area coated with photoresist and the other regions exposed. Dipping the sample in a solution of 1% hydrochloric acid solution for about 1-2 seconds was sufficient in etching the uncoated and exposed area of the film. Etching with HCl is so significantly fast that dipping a film sample for a few seconds is sufficient to etch even very thick films. After etching in HCl, the sample is rinsed and ultrasonically cleaned for 1 minute each in acetone, methanol, and IPA to completely strip off all coating of photoresist from the sample. Thereafter, the profilometer or AFM maps the step edge profile created to find the thickness.

Optical Interference

When a fraction of the light that is transmitted through the film is internally reflected before passing through the sample, a thin film interference occurs. The interference fringe pattern is produced due to the back and forth bouncing off the incident photons as it passes through the air-film-substrate interface. The result is either a constructive (maxima) or destructive (minima) interference effect on the film depending on the thickness and wavelength of the incident light. For ZnO film samples, the interference effects are observed as oscillations in the visible region on the spectral transmission curve. The thickness of the film can be estimated through these fringes by using the envelope method as proposed by Swanepoel [209].

$$d = \frac{N\lambda_a\lambda_b}{2(n_a\lambda_b - n_b\lambda_a)} \tag{3.16}$$

where λ_a and λ_b represent the wavelengths of two minima or maxima and N is the number of fringes between λ_a and λ_b, n_a and n_b are the refractive indices of ZnO at wavelengths of λ_a and λ_b respectively. This method was used to estimate the thickness of films with these fringes. A typical transmission spectrum of the ZnO sample with an interference fringe is shown in Fig. 3.12. Film thickness found by applying the method was $\approx$ 500nm. The drawback of this method was that accuracy was limited due to ambiguity in determining the exact position of the maxima or minima especially close to

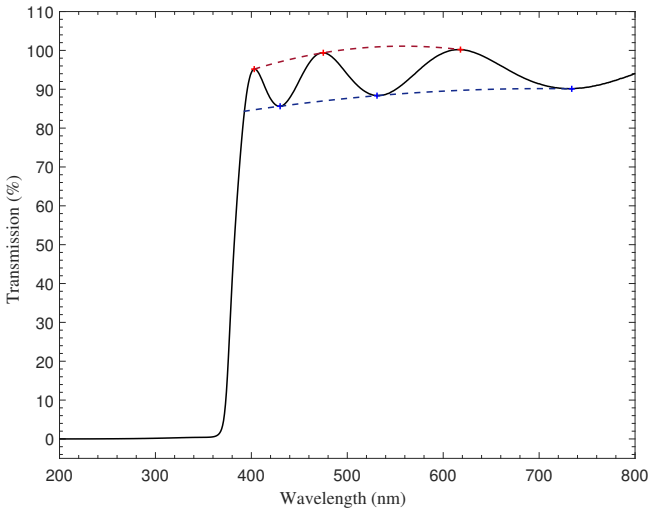


FIGURE 3.12: Transmission spectrum of a ZnO film sample showing interference fringes. The envelop method was used to estimate the thickness of the film using adjacent maxima.

the absorption edge. Moreover, the interference oscillation is observed for films with thickness above 200 nm. Only a few ZnO film samples were thick enough to allow for the envelope method as a routine method of finding film thickness. The use of the method was limited to only a few samples.

3.5 Summary

The mist-CVD film deposition system is one of the variants of the general CVD-based growth techniques. It allows the growth of ZnO and other oxide films under the atmospheric conditions without the need for a vacuum system and with safe precursor chemicals.

The deposition reactor in a mist-CVD technique can be of the hot wall or fine channel types. The very narrow channel in the fine-channel type enables improved uniform temperature distribution and ensures that enough growth species are supplied by concentrating the vaporized gas on the substrate.

There are two mechanisms available that explain the process of mist formation by ultrasound pulses - capillary wave model and cavitation. The well-accepted theory is the combination of both effects leading to mist formation.

Techniques utilized to study mist-CVD deposited ZnO films include the AFM for surface morphology, UV-Vis transmission and photoluminescence spectroscopy for optical characterization and Hall effect measurements for electrical studies. Crystalline properties were investigated using XRD while film thickness was determined with a profilometer after etching to form step edge on film sample.

Chapter 4

Mist-CVD growth of ZnO thin films

4.1 Introduction

This chapter presents the results of morphological and electrical characterization undertaken on mist-CVD deposited films. In particular, the chapter describes the use of aqueous ammonia as a precursor solvent. There is a discussion on the growth of ZnO films using a novel growth recipe which has not been reported previously. Aqueous ammonia serving as a precursor solvent eliminates some of the shortfalls associated with the use of volatile organic solvents such as methanol, acetone or IPA widely reported as solvents in the mist CVD growth of ZnO films. A safer recipe that does not comprise of volatile organic solvent in the growth of ZnO films has promising merits in terms of safety and applicability for high temperature growth of ZnO films.

There is a discussion on the surface structure of ZnO films examined through AFM in addition to the effects of some growth parameters such as precursor concentration and growth temperature. The results of electrical and crystalline properties of films studied through room temperature Hall effect measurement and x-ray diffraction (XRD) are discussed.

4.2 ZnO film Structure

The structure and morphology of a deposited film on a substrate is an important determining factor in its physical properties. Film morphology is affected by surface diffusion which is in turn controlled by factors such as substrate temperature, the partial pressure of gases and the overall total pressure of the system.

Generally, the structure of a deposited layer can be considered to be one of three types - epitaxial, amorphous or polycrystalline. A layer of film is considered epitaxial if it is a defect-free single crystal of a material deposited on the same material as substrate (homo-epitaxy) or on a different substrate (hetero-epitaxy). Epitaxial growth is in itself difficult and ideally occurs at high growth temperature and requires the substrate to be free from defects and other surface contaminants. Even for thin-film growth which may be considered epitaxial, it is often common for point defects and dislocations to be present in films [106]. Epitaxial growth of film is characterized by low growth rates to allow for the adsorbed species to move to low energy sites and mimic the surface structure of the underlying substrate. Epitaxial growth of film may be desirable in certain areas of application. For example, epitaxial layers of hafnium oxide or perovskite materials are more suitable in semiconductor applications in ferroelectric memory system, a form of random access memory technology with similar functionality as flash memory devices [200].

The amorphous type of film deposition typically occurs at low temperatures with a high growth rate leading to slow surface diffusion relative to the incoming precursor flux. For amorphous film nucleation, any form of crystallinity is prevented by the high number of the growth species such that after coalescence of the film, non-oriented grains with a complete absence of crystallinity are obtained [156]. Amorphous silicon is applied in solar cells and in thin film transistors for LCD displays.

In between the epitaxial and amorphous growth is the polycrystalline film structure. Polycrystalline films typically occur at intermediate temperatures forming islands of coalesced growth species with random orientation across the substrate. Polycrystalline films can be obtained more easily than epitaxial growths [156]. Polycrystalline semiconductor thin films find applications as conducting elements in circuits and devices as well as active conducting channel in thin film transistors, solar cells and detectors [214].

4.3 Substrate

It is common to find various works on epitaxial or polycrystalline ZnO films grown on c-plane (0001) sapphire substrates. Most of the growths report a polar c-axis oriented ZnO films as the preferred growth orientation, having an in-plane epitaxial relationship with (0001) sapphire substrate and other crystals of similar orientation e.g. (0001) CaF_2, (0001) $LiNbO_3$ [94]. However,

the microscopic field generated along the growth direction leads to polarization induced electric fields with the undesirable consequence for optoelectronic devices such as the reduction in the overlapping of electron and hole wave function and decrease in quantum efficiencies [77]. To eliminate the effects of polarization on ZnO, it is often advantageous to grow films with no polarization in the growth direction especially for optical and electronic devices. Several studies are reported on non-polar m-plane [122, 111] and a-plane ZnO film [69, 101] deposited on sapphire substrates mostly by MOCVD and molecular beam epitaxy. Obtaining $(10\bar{1}0)$ m-plane ZnO film is reported to be difficult with effects from other planes such as $(10\bar{1}3)$, (0002) and $(11\bar{2}2)$ included as minor planes during growth [43]. The choice of r-plane sapphire $(1\bar{1}02)$ substrate for majority of ZnO film samples as presented in this thesis stems from the above mentioned reasons. Additionally, sapphire substrates are relatively cheap, electrically insulating and transparent across the visible and near UV region with a bandgap of 9.9 eV. Another reason for the choice of the r-plane sapphire substrates is because, as discussed in section 4.6.3, smoother surface morphology with reduced roughness were obtained for ZnO films deposited on r-plane sapphire compared with c-plane sapphire substrates for depositions done in the same condition. Further, as explained above, a non-polar ZnO film is desirable for fabricating electronic devices since polarity effects that may degrade device performance are eliminated.

The chosen substrate has important implications in the growth process. Ideally, a homoepitaxial growth of the ZnO film of the desired crystal orientation on a ZnO substrate should be the best choice to obtain epitaxial films without substrate-induced strain. Single crystal ZnO wafers are however quite expensive with other issues such as possible damage to the surface during polishing [31] and migration of impurities from the substrate to the film during growth [146]. Growth of ZnO film on a substrate that is not ZnO implies a level of strain on the deposited film due to lattice mismatch between the substrate and a the film.

4.4 Novel Growth Recipe

One of the key aspects of the research was to investigate a safe precursor recipe applicable to mist-CVD growth of ZnO that does not rely on the use of organic solvents such as acetone, methanol or IPA. Many of the reports on ZnO related growth with mist-CVD have used precursor made of zinc acetate, zinc acetylacetonate or zinc chloride dissolved in pure methanol [97,

96], methanol-water mixture at 9:1 ratio [201], acetone-water mixture [176] or pure IPA [102]. In a few research works that used deionized water as the solvent, a low growth rate was reported [104]. Film uniformity is degraded by grains that are not dense and continuous across the substrate with optical characteristics from photoluminescence spectroscopy showing strong defect band in the crystal [42].

The dependence on organic solvents for reliable ZnO film nucleation on a substrate presents a risk of explosion and flammability since most organic solvents are volatile and flammable and may not be practical especially in an industrial scale with a need for high throughput. For instance, methanol has a flash point temperature of 12°C and an auto-ignition temperature of 385°C [148] which poses a serious fire risk at even moderate growth temperatures. Likewise, development of a growth recipe free from volatile organic solvent with desirable surface morphology, electrical and crystalline properties will be of interest for upscaling and industrial applications in terms of safety.

Based on experimental trials, a growth recipe for mist-CVD ZnO films that does not require a volatile organic solvent, was found in the course of my research. Unlike the attempt of Kawahamura [104] where an improved growth rate was achieved using methyl acetate in place of water, we found out that diluted aqueous ammonia provides key advantages both in atomization of liquid precursor and in the crystallization of ZnO. Apart from some mild reactions such as irritation to the skin and eyes, the handling and exposure to aqueous ammonia do not pose any serious medical health risk. Besides, proper protection in the form of a fume hood/extraction fan is used in a mist-CVD system to avoid any exposure. Aqueous ammonia of approximately 30% concentration by volume is rated with a slight flammability risk and is not absorbed through the skin. Further dilution with de-ionized water almost removes any risk of flammability. The use of aqueous ammonia instead of the commonly used organic solvent could allow for industrial and large scale mist-CVD facility without risking safety and potential risks to explosions associated with organic solvents. The next section discusses the role of aqueous ammonia in the mist-CVD growth of ZnO films.

4.4.1 Role of Ammonia

Ammonia was found to play an important role in the entire mist-CVD growth deposition process. There are two key contributions of aqueous ammonia in the growth process of ZnO films using the mist-CVD technique. Based on

visual assessment, aqueous ammonia is found to significantly improve the atomization of the precursor solution even for solutions with a high concentration of zinc acetate compared to deionized water. An illustration is seen in Fig. 4.1 which compares ultrasonic atomization of 0.1 M concentration of zinc acetate dehydrate dissolved in (a) de-ionized water and (b) aqueous ammonia. It is observed that atomization did not occur in the solution with deionized water as a solvent when subjected to ultrasonic pulses for 10 minutes. An explanation for the difference is that atomization of the precursor solution is dependent on its physical properties such a density, viscosity and surface tension in addition to the frequency and intensity of the ultrasound pulses. Increase in the concentration of zinc acetate in the solution leads to an increase in its density. A high density precursor solution reduces the capacity of the ultrasonic pulses to form mist out of the solution. A precursor solution that contains aqueous ammonia instead of only deionized water has the improved capacity to form mist particles by ultrasonic atomization due to reduction in the surface tension and density of the liquid solution[112]. Thus, aqueous ammonia as a solvent provides the means to atomize precursor solutions with high concentration of zinc acetate salt which may normally be impractical with deionized water only. Further, aqueous ammonia has also been noted to act as surfactants in the MOCVD growth of ZnO [22]. It was observed that with deionized water as solvent, atomization and mist formation from precursor concentration of 0.05 M and above is mostly impractical.

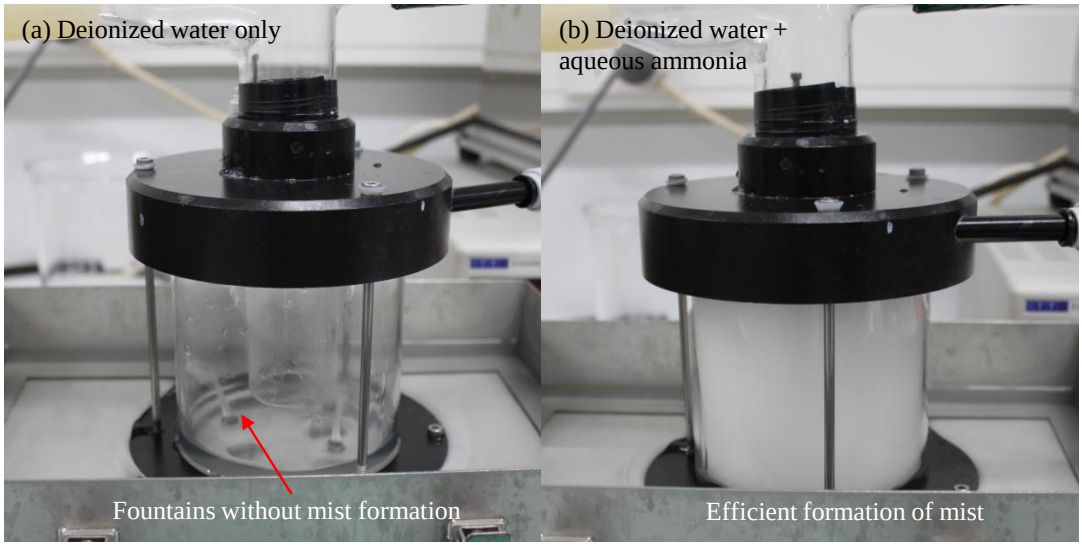


FIGURE 4.1: Photographic images showing 0.1 M precursor solution of zinc acetate dihydrate dissolved in (a) deionized water and (b) deionized water and aqueous ammonia mixture (5% v/vol) after 10 minutes of atomization.

Another important benefit of using aqueous ammonia is in the crystallization process of ZnO. It has been reported that aqueous ammonia allows for a fast, low energy reaction in the dissociation of complex zinc amines (discussed in section. 6.4) and further dehydration that leads to the formation of crystallized ZnO [99]. Furthermore, Zn^{2+} acting like other Lewis acids readily forms amine complexes with ammonia in an aqueous environment. Ammonia is particularly different from other nitrogen-based ligands by its volatility and ability to form reactive and transient chemical species, allowing low temperature and rapid decomposition process to form ZnO [150]. This benefit is supported in the pH dependence growth of ZnO films where a dramatic increase in growth rate was observed when aqueous ammonia is used as a solvent. A low growth rate was noticed when only de-ionized water was used as a precursor solvent, an observation that has been confirmed by other researchers [104].

It was found from my work that with aqueous ammonia as the solvent, zinc acetate dihydrate as the zinc source and the precursor solution at a basic pH, dense and uniform ZnO films were deposited on various substrates. Oxygen gas was used as both the carrier and dilution gas for all growths of ZnO films. The use of oxygen gas was necessitated by the report of Burgett *et al.* [22] which suggests that the three excess hydrogen atoms available with the dissociation of ammonia tend to become trapped in the crystalline structure of ZnO. Hydrogen atoms can potentially passivate the electrical activity in many deep level defects and impurity states as well as surface dangling bonds [181]. Another reason for the use of oxygen gas flow during the growth process is to compensate for the excess nitrogen and reduce oxygen vacancies.

4.5 ZnO film crystallization

All of the ZnO films presented in this thesis were grown with zinc acetate dissolved in aqueous ammonia solution. One important parameter that controls the growth of ZnO film is the volume of aqueous ammonia present in precursor solution which in turn determines the pH of the precursor. We outline the supposed chemical interaction routes in a mist-CVD process that results in the crystallization of ZnO via zinc acetate dissolved in aqueous ammonia solution.

Equations 4.1 - 4.3 describe the hydrolysis of ammonia and the dissociation of zinc acetate dehydrate in the presence of deionized water. In aqueous

solution, zinc acetate dehydrate dissociates to zinc ions, Zn^{2+} and acetate ions, CH_3COO^-. Further hydrolysis of the acetate ions produces OH^- ions as shown in reaction Eqn. 4.3.

$$NH_3 + H_2O \longleftrightarrow NH_4^+ + OH^- \tag{4.1}$$

$$Zn(CH_3COO)_2 \rightarrow 2CH_3COO^- + Zn^{2+} \tag{4.2}$$

$$CH_3COO^- + H_2O \rightarrow OH^- + CH_3COOH \tag{4.3}$$

The reaction of Zn^{2+} ions with NH_4^+ and OH^- results in the formation of zinc amine complexes such as tetra-aminezincate ions $Zn(NH_3)_n^{2+}$, zinc hydroxide $Zn(OH)_2$ or tetra-hydroxozincate ions $Zn(OH)_4^{2+}$ as shown in the reactions of Eqns. 4.4 - 4.6. These zinc amine complexes are considered ZnO intermediates since they are important components in transforming to ZnO structures.

$$Zn^{2+} + 2OH^- \rightarrow Zn(OH)_2 \tag{4.4}$$

$$Zn^{2+} + 4OH^- \rightarrow Zn(OH)_4^{2-} \tag{4.5}$$

$$Zn^{2+} + 4NH_4^+ \rightarrow [Zn(NH_3)_4]^{2+} \tag{4.6}$$

These intermediate zinc-amine complexes undergo further reactions leading to crystallization and nucleation of ZnO. The reaction between $[Zn(NH_3)_4]^{2+}$ complex amine with OH^- yields ZnO. Additionally, dehydration of zinc hydroxide $Zn(OH)_2$ leads to the formation and crystallization of ZnO nuclei based on reaction Eqns. 4.7 - 4.9.

$$[Zn(NH_3)_4]^{2+} + 2OH^- \rightarrow ZnO + 4NH_3 + H_2O \tag{4.7}$$

$$Zn(OH)_4^{2-} \rightarrow ZnO + H_2O + 2OH^- \tag{4.8}$$

$$Zn(OH)_2 \rightarrow ZnO + H_2O \tag{4.9}$$

The stability of these complexes is dependent on the pH and temperature of the solution [227]. The chemical reactions above that describe the crystallization of ZnO, are based on various reviews of different works on the formation of ZnO from sol-gel and other wet chemical methods that utilized zinc acetate. Although a proposed chemical reaction route taking place has been outlined, it will be necessary to mention that the formation of ZnO from aqueous solution is a complex reaction process. Many complex cationic species can be formed from the reaction between Zn^{2+} and OH^-, and is dependent on the pH, temperature and method of growth [195]. A complete

understanding of the exact chemical reactions and the exact complex amine specie that leads to the crystallization of ZnO may require advanced chemical analyses which may be superfluous as to the goal of this research. However, the proposed zinc amine mediated chemical route where zinc amine complexes play a key role as ZnO intermediates is the most reasonable reaction mechanism taking place in the reaction process. It is typical to find chemical reactions describing the formation of ZnO nanostructures in alkaline solution of zinc acetate using $Zn(OH)_2$ and $Zn(OH)_4^2$ amine mediated growth units. This hypothesis is strongly supported in the report of Park *et al.* [177].

Our experimental results show that ZnO film is formed even with moderate addition of aqueous ammonia in deionized water. Our attempt to grow ZnO with only water as solvent at low concentration did not yield practicable result as the growth rate was too low. Conversely, an attempt to grow with water only solution at a higher concentration of zinc acetate in solution was not practical as an increased precursor density at high concentration limited to a large extent the capacity to atomize the liquid precursor via ultrasound, with no films deposited.

4.6 Results/Discussion

Growth of thin layers of ZnO was successfully deposited on substrates including sapphire and amorphous quartz. Film deposition was typically done on a 10 mm $\times$ 10 mm area. For characterization techniques such as Hall effect measurements or photolithography for device fabrication, the deposited ZnO film sample is usually diced using a wafer saw to 5 mm $\times$ 5 mm samples. A standard deposition condition for the growth of ZnO film is shown in Table 4.1. The pH of the aqueous ammonia solution measured before the

TABLE 4.1: Standard growth conditions for mist-CVD deposited ZnO films

Growth Temperature	500°C
Substrate	Al_2O_3
Carrier gas	O_2
Precursor pH (aqueous ammonia)	12.60 $\pm$0.05
Flow rate	10 lit/min (carrier + dilution)

addition of zinc acetate salt was kept constant for all growths presented in this thesis. Some of the properties of deposited ZnO films and the effect of growth parameters are discussed next.

4.6.1 Growth rate and film thickness

There are basically three key factors that affect the growth rate of ZnO films - deposition temperature, precursor concentration and pH. Initial experimental investigations were carried out to determine optimal conditions for the growth of ZnO films. The effect of temperature on growth rate was initially carried out by depositing ZnO films on r-plane sapphire substrates at different growth temperatures. Variation in the growth rate as a function of deposition temperature is shown in Fig. 4.2(a). Growth rate was maximum for a sample grown at a temperature of 300°C. The average growth rate was determined to be 3 nm/min at 300°C which reduced to 1.2 nm/min at 400°C and eventually increases to 2.4 nm/min at a substrate temperature of 550°C. The high growth rate for the sample grown at 300°C is due to the temperature

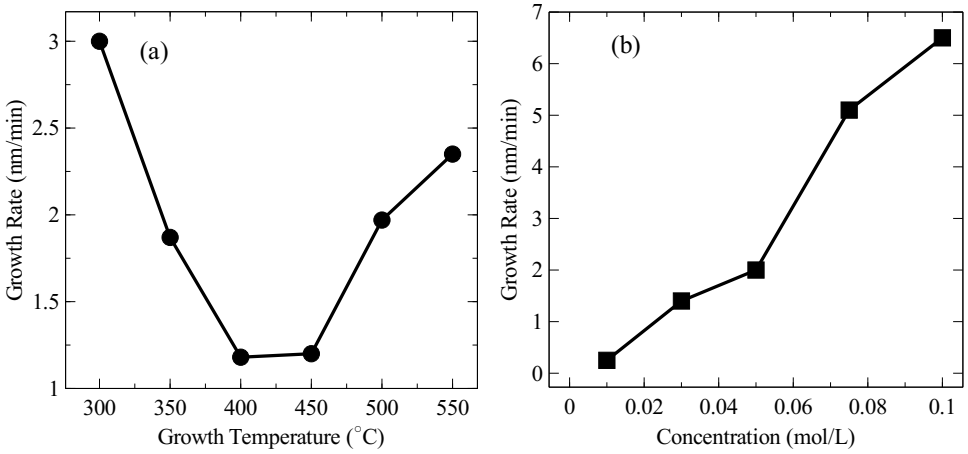


FIGURE 4.2: (a) Graph showing the variation of growth rate with substrate temperature from 300 - 550°C at a concentration of 0.05 mol/L (b) Variation of growth rate at varying precursor concentration.

not being sufficient for a complete precursor decomposition. Film nucleation with incomplete vaporization of mist droplets is characterized by the formation of unstable vapor, deposition of precursor molecule, wetting of substrate and a resultant formation of thick layers of inhomogeneous film on the substrate [169]. These factors contribute to degradation of film nucleation and quality. Additionally, as represented in the plot of Fig. 4.2(b), increase in precursor concentration results in higher growth rate due to increased amount of growth species available for nucleation.

The plots in Fig. 4.2 represent results of initial experimental trial with the aim of finding optimal growth temperature and concentration that will yield good quality films. However, experimental uncertainties which can be estimated by performing the repeated experiments are not taken into account.

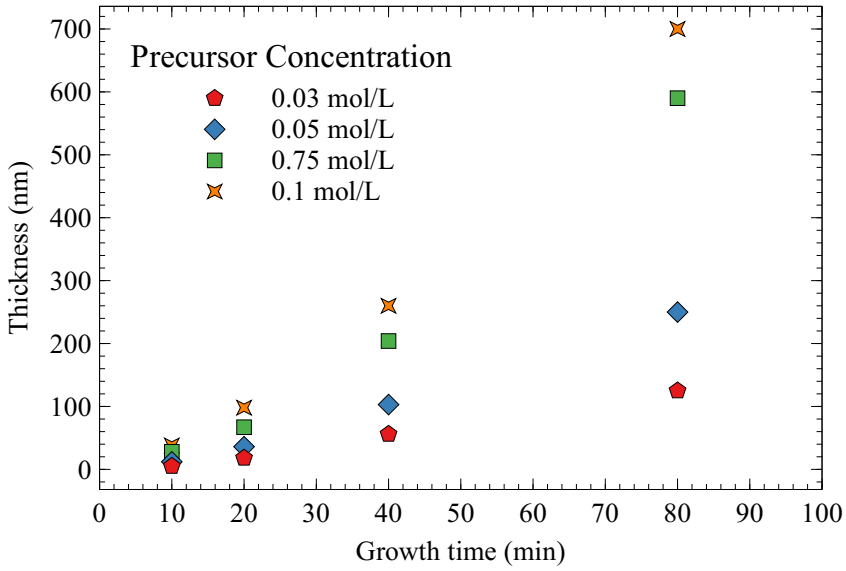


FIGURE 4.3: Plot showing the variation of film thickness with growth time for ZnO films grown at 500°C at different concentration of precursor solution.

Also, measurement uncertainties in finding the thickness of film by etching and measuring a step edge profile across the film is not represented in the plot.

An attempt to deposit ZnO film below a growth temperature of 300°C was not investigated, since, the characteristics of film sample grown at 300°C are degraded in film quality. For the stated reasons arising from the decomposition temperature of zinc acetate, it is reasonable to conclude that growth of ZnO films below 300°C using our mist-CVD system and recipe is unlikely to yield films of improved quality.

A scatter plot of film thickness vs. growth time at a varying concentration of precursor solution is shown in Fig. 4.3. As expected, both the growth time and precursor concentration are found to increase the thickness of films deposited on the substrate. The plot shows a non-linear relationship between film thickness and precursor concentration. For instance, doubling the concentration from 0.05 mol/L to 0.1 mol/L increased film thickness from about 105nm to 260 nm for film samples grown for 40 mins duration. Similar non-linear trend in growth rate with precursor concentration is observed for films grown for 80 mins. This observation may be explained by the rapid nucleation at higher concentration due to increased growth species. The growth rate at 0.01 mol/L was very small and was not included in the plot.

Another important factor that affects the growth rate of films is the pH of the precursor solution. The addition of aqueous ammonia increases the pH

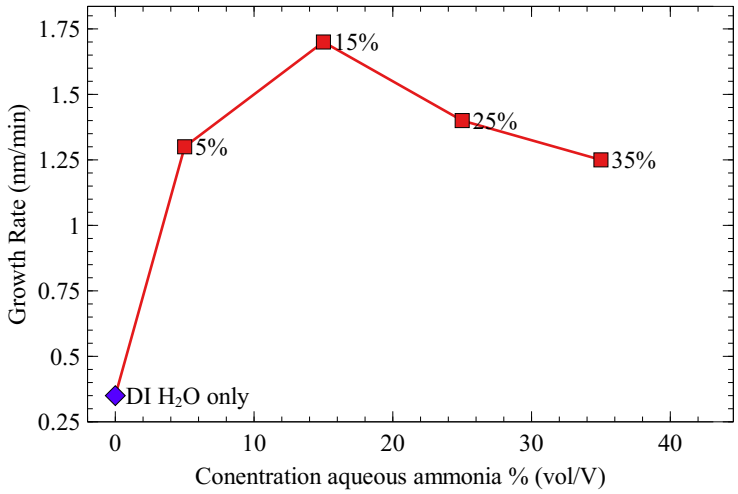


FIGURE 4.4: Variation in growth rate of ZnO films deposited at 500°C for precursors made of deionized water only and aqueous ammonia at different concentrations.

and makes the precursor solution more alkaline. The more aqueous ammonia in solution, more OH^- and NH_4^+ ions are available for the formation of ZnO based on the reaction equations outlined in the previous section. The initial preliminary investigation was undertaken to find the optimal pH for the growth of ZnO films using the mist-CVD system. ZnO films were grown at a precursor concentration of 0.03 mol/L on a sapphire substrate. The concentration of aqueous ammonia in the precursor solution was varied between 5% - 35 % (v/v%). Growth was also done with only deionized water as a solvent. By indirectly varying the pH of precursor by the fractional volume of aqueous ammonia in solution, an optimal pH was found for the precursor which gave the maximum growth rate. These experimental findings were carried out at the initial stages of the research project, aimed at finding an optimal growth condition for subsequent growth of films. As shown in Fig. 4.4, there was a dramatic improvement in the growth rate with the use of aqueous ammonia as a solvent compared with deionized water only. Growth rate of between 1.25 nm/min to 1.7 nm/min was achieved at 5% - 35 % (volume percent) of aqueous ammonia in precursor concentration. For consistency and reproducibility, a calibrated pH meter was used to measure the pH of a $\sim$ 15% precursor solution which gave a pH value of 12.60$\pm$0.05. This pH was maintained for later growths of ZnO films reported in this thesis.

4.6.2 Crystalline Properties

The θ-2θ XRD patterns for ZnO films grown on r-plane, c-plane, and a-plane sapphire substrates are shown in Fig 4.6. For the film sample grown on r-plane sapphire substrate, the two prominent peaks in the pattern are from the $Al_2O_3(20\bar{2}4)$ sapphire substrate and ZnO($11\bar{2}0$) peak centered at 2θ angle of 56.64°, indicating preferred growth of non-polar a-plane ZnO film with an orientation relationship of $(11\bar{2}0)_{ZnO}$ // $(10\bar{1}2)_{sapphire}$. An illustration of atomic arrangement of a-plane ZnO surface and r-plane sapphire substrate is shown in Fig. 4.5. From the schematic diagram, the lattice mismatch considering the in-plane translational periodicity along the m-direction $[1\bar{1}00]_{ZnO}$ and c-direction $[0001]_{ZnO}$ is 18.3% and 1.55% respectively. This small lattice mismatch along the c-direction is attributed to the elongated grain morphology and formation of striation along the c-axis ZnO[0001] direction [172] for ZnO films grown on r-plane sapphire (see section 4.6.3). The diagram on the right side of Fig. 4.5 shows a more intuitive orientation of a-plane ZnO with respect to r-plane sapphire substrate. This observed preferential growth orientation agrees with other reports of ZnO films deposited on r-plane sapphire which tends to have a preferential a-axis orientation [77, 43].

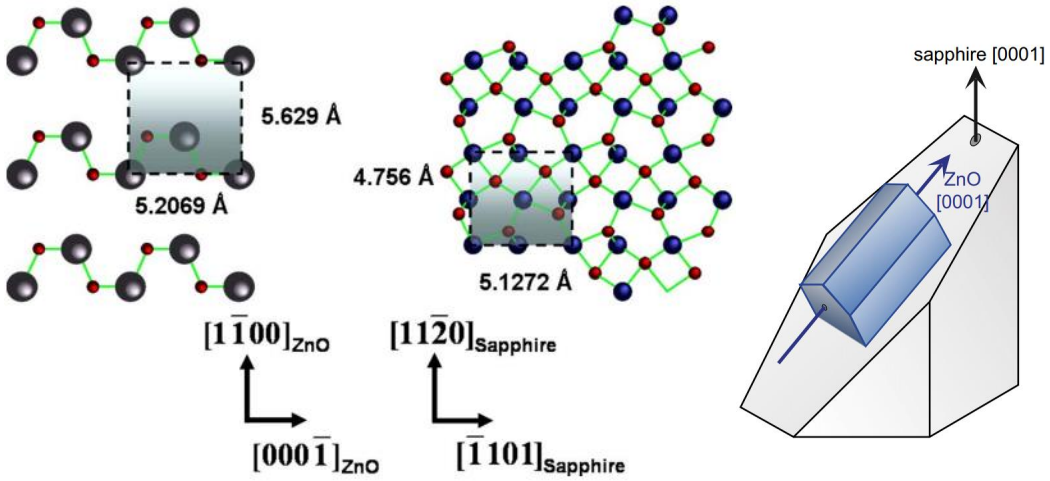


FIGURE 4.5: Schematic representation of surfaces of a-plane ZnO and r-plane sapphire substrate with rectangles indicating the surface unit cell and associated in-plane lattice parameters.

For film depositions on c-plane substrates, the intensity of the ZnO(0002) peak centered at a 2θ diffraction angle of 34.42° dominates that from the sapphire substrate. The relatively strong ZnO(0002) peak indicates that the preferred growth orientation is the c-axis. These results are consistent with several articles in the literature confirming (0001) preferential orientation of ZnO

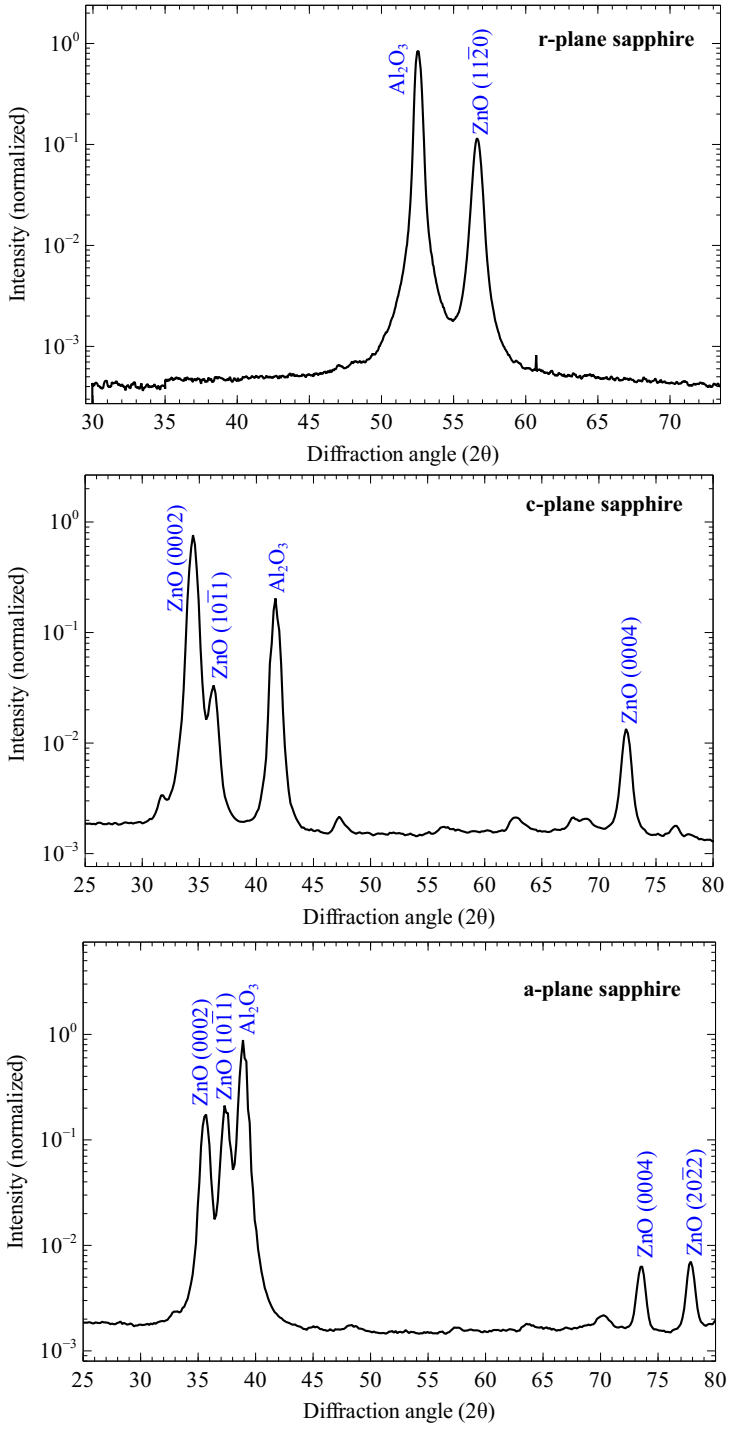


FIGURE 4.6: X-ray diffraction pattern for ZnO films deposited on sapphire substrates of different crystallographic planes.

films for growths on a c-plane sapphire substrate. A schematic diagram illustrating atomic positions for ZnO growth on c-plane sapphire substrate is shown in Fig. 4.7.

The lattice mismatch existing between ZnO and the underlying c-plane

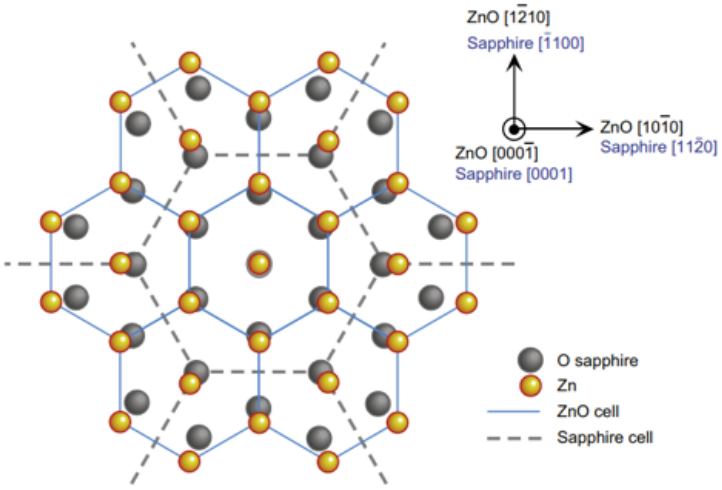


FIGURE 4.7: Schematic diagram showing atomic arrangement of basal ZnO[0001] oriented film grown on c-plane (0001) sapphire substrate with their epitaxial relationship. The dashed and solid lines represent the boundaries of sapphire and ZnO unit cells respectively [174].

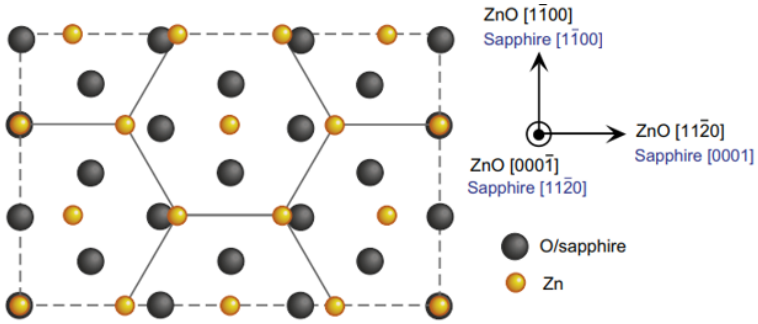


FIGURE 4.8: Schematic diagram showing atomic arrangement of basal ZnO[0001] oriented film grown on a-plane (11$\bar{2}$0) sapphire. The lattice parameter a of ZnO is almost 1/4th of c lattice parameter of sapphire with a mismatch of less than 0.08% [174].

sapphire substrate is as high as 32% which can be reduced to 18.4% with in-plane 30° rotation. Despite the reduction in lattice mismatch with the underlying sapphire, there is a possibility that this causes as-grown ZnO to have high mosaicity and low carrier mobilities, thereby limiting applications of ZnO[0001] oriented ZnO for optoelectronic applications [172].

The presence of ZnO(0004) diffraction peak at 2θ angle of 72.50° secondary to the ZnO(0002) direction indicates that good quality crystal can be achieved even with this cost-effective growth method. There is an observable poly-crystallinity with diffraction peaks from the ZnO(10$\bar{1}$1) shown on the spectrum, though with diminished intensity. It is of note that (10$\bar{1}$1) is a high atomic density crystal plane with some reports of ZnO(10$\bar{1}$1) peak

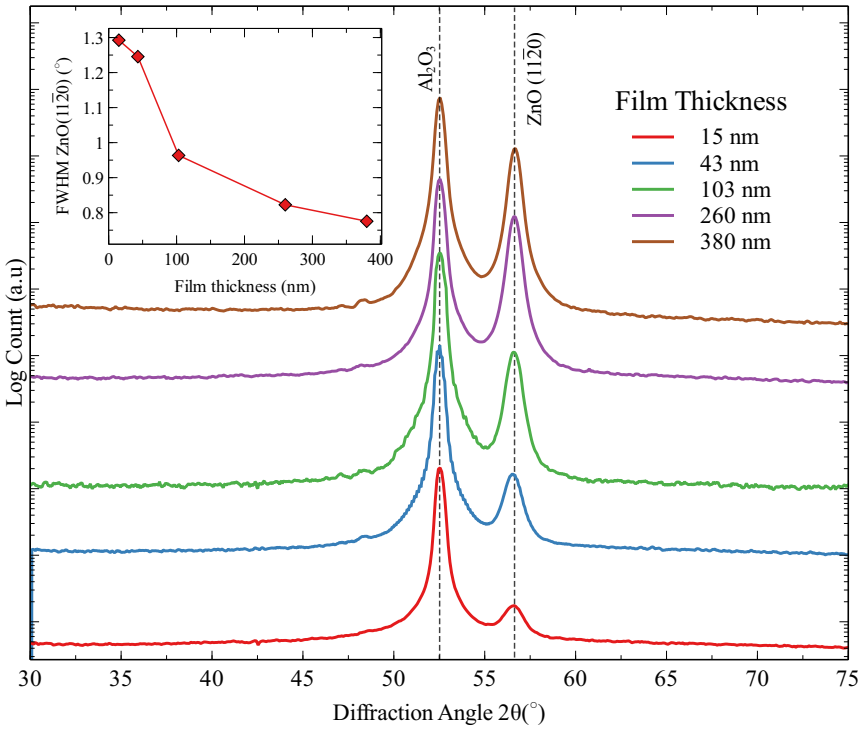


FIGURE 4.9: Diffraction pattern of ZnO films of various thicknesses deposited on r-plane sapphire substrate. Vertical offset is applied to y-axis for for clarity. Inset - Changes in FWHM for ZnO(11$\bar{2}$0) peak with increase in film thickness.

simultaneously observable alongside a ZnO(0002) peak in some ZnO films with c-axis growth orientation [184]. Some contributing factors associated with the presence of (10$\bar{1}$1) peak in ZnO nanostructures with normally (0002) preferred growth orientation include low substrate temperature [252] and stress on films [6].

Growth on a-plane sapphire shown in Fig. 4.6 has two main peaks originating from the film. On the XRD pattern, reflection peaks from ZnO(0002) and ZnO(10$\bar{1}$1) are observed with comparable intensities. Our XRD pattern is almost similar to the observation reported by Xie *et al.* [242] on epitaxial ZnO film deposited on a-plane sapphire using chemical vapour deposition technique. As illustrated in the schematic diagram in Fig. 4.8, a prominent c-axis orientated ZnO film on a-plane sapphire substrate is based on the background that a 4-fold of a lattice constant in ZnO (4 $\times$ 3.249 Å= 12.996 Å) fits perfectly to the c lattice constant of sapphire (c = 12.99 Å) with a mismatch of less than 0.08% at room temperature. This small mismatch is behind the expected preferential growth of c-axis orientated ZnO film on an a-plane sapphire substrate. The additional (10$\bar{1}$1) peak is commonly observed for ZnO films and nanowires grown on a-plane sapphire substrate [231, 197, 242].

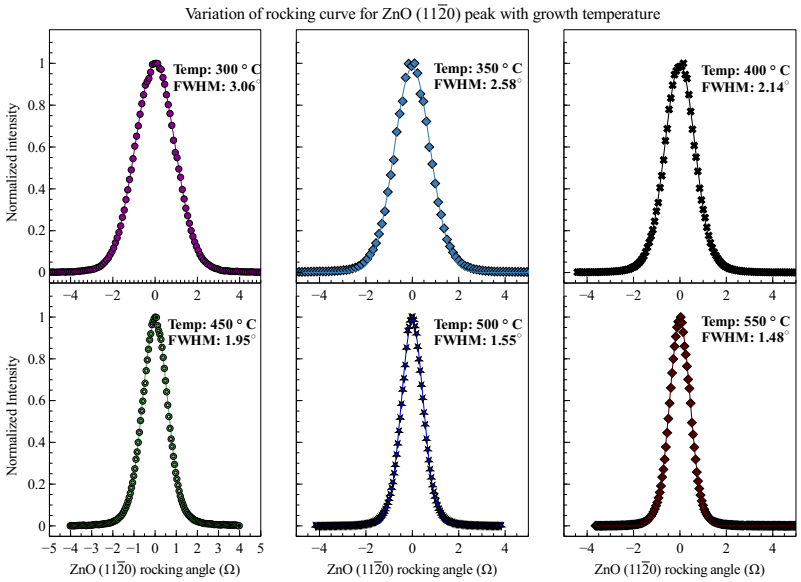


FIGURE 4.10: Rocking curve analyses for the ZnO (11$\bar{2}$0) diffraction peak showing decrease in the FWHM as growth temperature increases. Thickness of film samples is approximately 80 - 100 nm.

A plot of θ-2θ diffraction pattern for ZnO films of different thicknesses deposited on r-plane sapphire substrates is shown in Fig. 4.9. The plots show that the relative intensity of the ZnO(11$\bar{2}$0) diffraction peak becomes higher as the film thickness increases. Similarly, there is reduction in broadening profile from ZnO(11$\bar{2}$0) peak with increase in the thickness of film. The inset plot shows the instrument dependent FWHM of a 15 nm thick film to be 1.3 ° which reduced to 0.8 ° for a film of 260 nm thickness. There is no noticeable shift in the 2θ diffraction angle with changes in the film thickness.

Rocking curve analyses performed on the ZnO(11$\bar{2}$0) peak at different growth temperatures shown in Fig. 4.10 indicate an improvement in the crystalline properties of films at higher growth temperatures with the narrowing of the peaks when growth temperature increased. The lowest FWHM was obtained for the film deposited at 550°C whereas, for the film sample deposited at 300°C, the FWHM was about two times that of 550°C growth temperature.

ZnO being a hexagonal structure with inter-planer distance d_{hkl} is related to the lattice constants a, c, and the Miller indices $h\ k\ l$ by the relation [37],

$$\left(\frac{1}{d_{\mathrm{hkl}}}\right)^2 = \frac{4}{3}\left(\frac{h^2+hk+k^2}{a^2} + \frac{l^2}{c^2}\right) \tag{4.10}$$

The ZnO(0002) diffraction peak centred at a 2θ angle of 34.42° and ZnO($11\bar{2}0$) peak at a 2θ angle of 56.5° are used to calculate the c and a lattice parameters using the relation $\lambda / \sin\theta$, derived from Eqn. 4.10. The c lattice constant was found to be 5.207 Å which is close to the reported value 5.213 Å for the bulk ZnO [173]. Similarly, calculated a lattice constant gave a value of $a = 3.254$Å, very close to the a lattice constant of 3.252 Å for the bulk.

The XRD analyses also provide a way to evaluate the the crystallite size using the peak broadening of the diffraction peaks. Diffraction peak broadening is determined by both the contributions of the instrument and crystalline structure of the sample. The instrument corrected structural broadening arising from the sample is estimated using the relation [188],

$$\beta_f = (\beta_h^2 - \beta_g^2)^{1/2} \tag{4.11}$$

where the subscripts f, h and g represent the structural, measured and instrumental broadening profiles respectively, quantified as FWHM of diffraction peaks. A standard peak from the sapphire substrate was used to represent the broadening effect from the instrument.

The average crystallite size was calculated from ZnO($11\bar{2}0$) peak using the Scherrer formula [188],

$$D = \frac{K\lambda}{\beta_f \cos\theta} \tag{4.12}$$

where D is the average crystallite size, K is the shape factor that is close to unity with value typically taken as 0.9, λ is the wavelength of incident x-ray (1.540 Å), and θ is the Bragg angle. The average crystallite size for a 15 nm thick film is found to be $D \sim$15 nm while for a film with thickness of 380 nm, average crystallite size is approximately 19 nm and monotonically increases with film thickness.

It is of note that the Scherrer relation in Eq. 4.12 assumes that the peak broadening in the XRD pattern results only from the size of the particles. Additionally, peak broadening can arise due to the strain ϵ induced by crystal imperfection and is quantified using the relation,

$$\epsilon = \frac{\beta_f}{4\tan\theta} \tag{4.13}$$

If strain-induced contribution to line broadening is considered, the observed line width is the sum of Eqns. 4.12 and 4.13.

$$\beta_f = \frac{K\lambda}{D\cos\theta} + 4\epsilon\tan\theta \tag{4.14}$$

which is rearranged to be in the form

$$\beta_f \cos\theta = \frac{K\lambda}{D} + 4\epsilon \sin\theta \tag{4.15}$$

The above relation is Williamson-Hall equation [157] where a plot of $\beta_f \cos\theta$ against 4sin θ for all diffraction peaks is used to find the crystallite size and strain from the intercept and slope respectively. Williamson-Hall analyses can be applied to powder sample or polycrystalline films with multiple growth orientations in the diffraction peak pattern which will allow sufficient data points for a linear fitting. However, this model may not apply to the XRD patterns of film samples represented in Fig. 4.9 since growth is preferential along a particular crystalline direction with only a single diffraction peak from the film. If the contribution to the peak broadening due to strain is considered, it can be inferred that strain is reduced with an increase in film thickness.

4.6.3 Film Surface Morphology

The surface morphology of deposited thin films of ZnO was studied using AFM. The variation in the surface morphology of films with thickness ranging between 80 nm - 100 nm deposited at growth temperatures from 300 - 550°C is shown in Fig. 4.11. For a film sample deposited at 300°C, it appears that the film was not compact with no well-defined grains and possibly of some residue on the substrate. A probable reason for such film morphology at 300°C is an incomplete thermal decomposition of the precursor solution or the intermediate products which may have caused wetting and deposition of precursor residue. Film surface topography improved at a growth temperature of 400°C with R_{rms} = 2.4 nm. As growth temperature increases up to 500°C, agglomeration of multiple grains into elongated structures is observed with increased surface roughness of films up to R_{rms} = 3.7 nm at 550°C. The average grain size of 58 nm was found for film grown at 550°C with each grain delineated through a threshold algorithm available with Gwyddion [73].

The growth rate and surface roughness were maximum for the sample grown at 300°C which is also attributed to the fact that incomplete decomposition, wetting of substrate and other factors associated with the formation of unstable vapor at this temperature contributed to degrading the film quality. In terms of electrical properties as shown in table 4.2, the sample deposited at 300°C was the most resistive ZnO film sample among other samples of similar thickness grown at a higher temperature. The marked difference in film

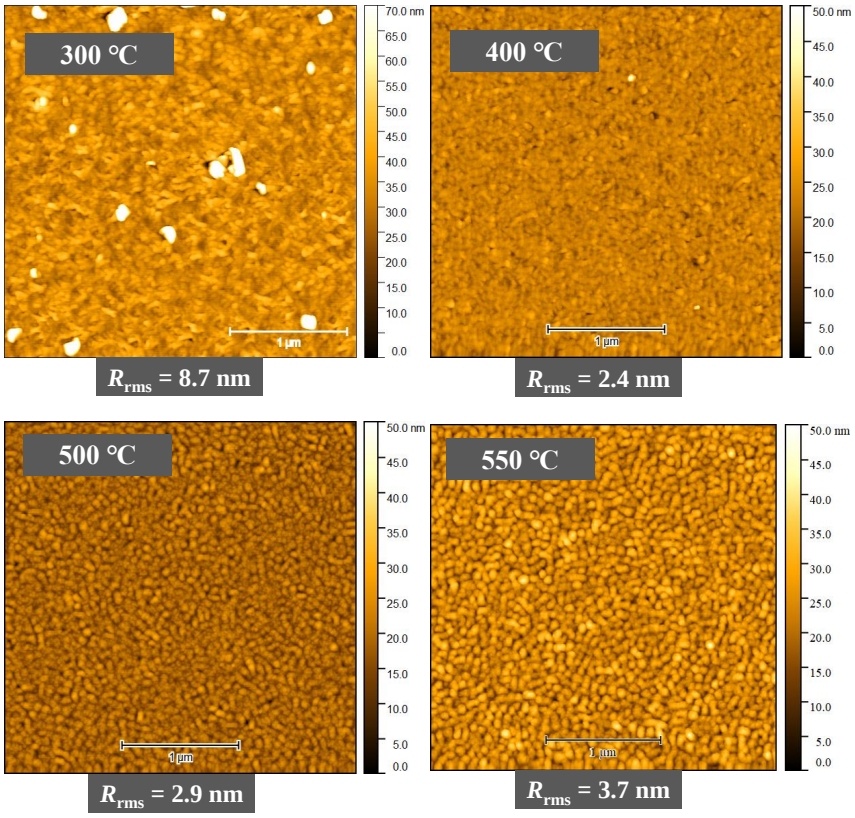


FIGURE 4.11: Surface morphology of ZnO film samples approximately between 80 - 100 nm in thickness deposited with a precursor concentration of 0.05 mol/L at different growth temperatures.

surface morphology for film sample grown at 300°C and others deposited at higher temperatures agrees with several reports on thermogravimetric analyses of zinc acetate which show that formation of ZnO occurs from a decomposition temperature of ∼315°C and above [202].

An investigation of how the concentration of precursor solution affects the surface morphology of ZnO films deposited at 500°C is shown in Fig. 4.12. It is observed that the grains were deposited uniformly on the substrates at different concentrations investigated. It is also observed that the grains for growth at a relatively low concentration of 0.01 mol/L were well-defined and isolated. As the concentration of the precursor increases, the grains increasingly become coalesced together into larger grains and elongated as observed for growths done at concentration of 0.05 - 0.15 mol/L. With an increase in precursor concentration, the number of growth species that leads to film nucleation increases as well as the electrostatic interactions raising the probability of forming larger grains [48]. At low precursor concentration, the relatively reduced amount of growth species gives time

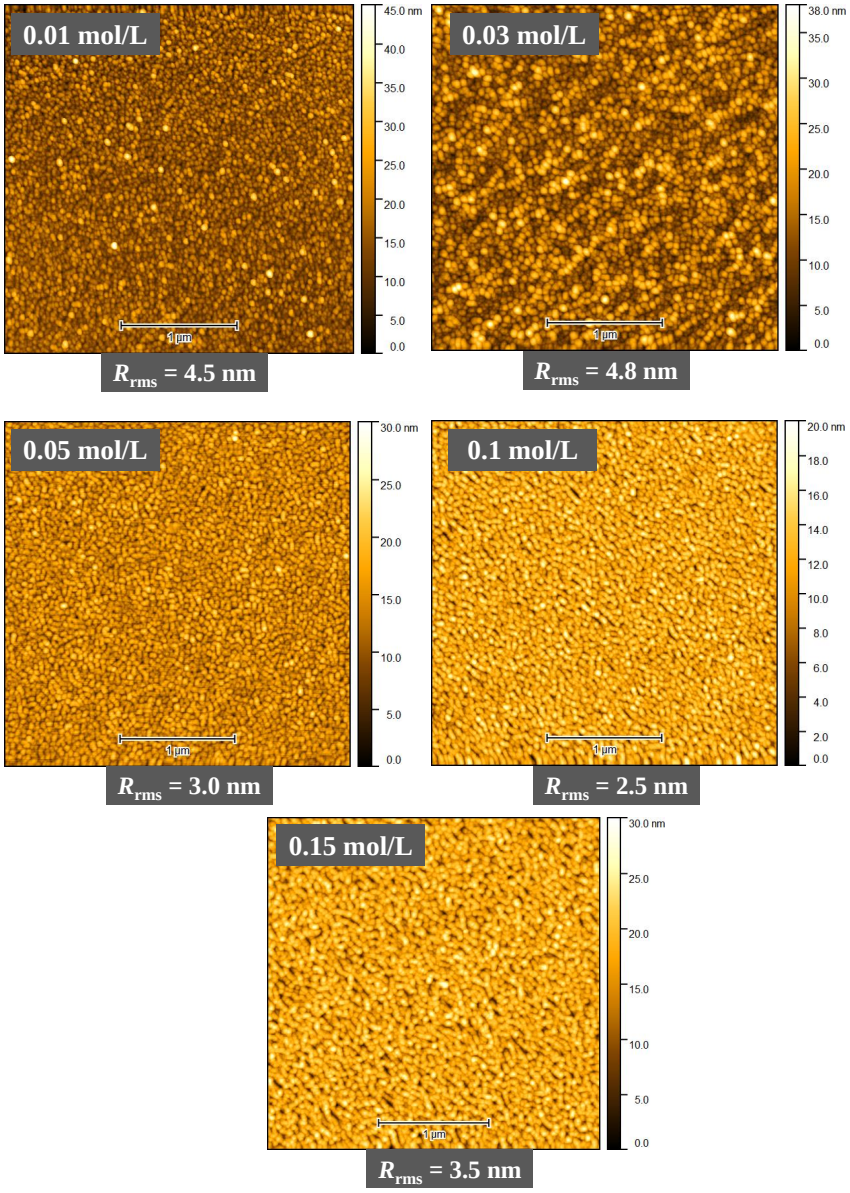


FIGURE 4.12: Variation of surface morphology for ZnO films with thickness ranging between 45 - 65 nm deposited at 500°C with varying precursor concentration on r-plane sapphire.

for complete nucleation before the arrival of subsequent species. However, at higher precursor concentration, high amount of growth species available for nucleation entails that there is less time for subsequent arrival of growth species leading to agglomeration of the grains.

Surface morphologies of ZnO films grown on r-plane sapphire substrates at a precursor concentration of 0.1 mol/L at 500°C for varying growth times are shown in Fig. 4.13. Growths on r-plane sapphire substrate at 5 mins duration show that at the onset of film growth, coverage across the substrate was uniform with grains coalesced together to form elongated grains. As

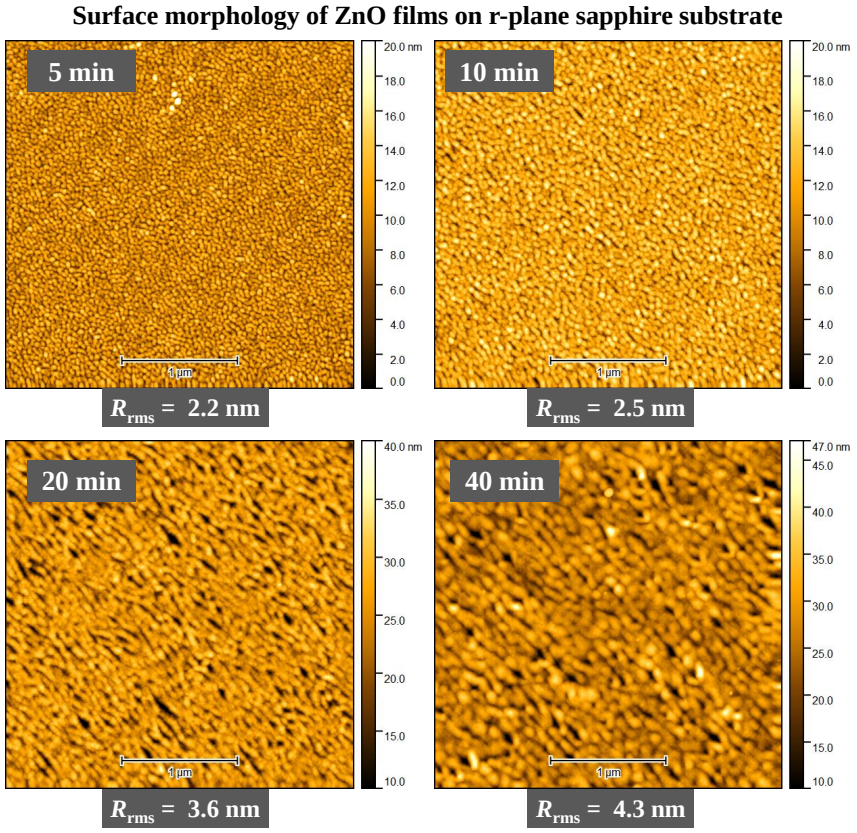


FIGURE 4.13: Surface morphology of ZnO film samples deposited at a growth temperature of 500°C and concentration of 0.1 mol/L on r-plane sapphire substrates at different growth times.

the thickness of films increases with longer growth times, the amalgamation of grain structures become more noticeable and aligns diagonally in the c-axis direction ZnO[0001] along with atomic steps of r-plane sapphire. The existence of such atomic steps has been observed on a bare r-plane sapphire substrate [32]. Similar anisotropic morphology with strips elongated along the c-axis is reported for non-polar ZnO films grown on r-plane sapphire substrate [43]. Film roughness increases with increase in growth time and resultant increase in thickness. Analyses of AFM images for surface roughness show that ZnO films deposited on r-plane sapphire for 5 min has R_{rms} = 2.2 nm, and R_{rms} = 2.5 nm for a 10 mins growth time. Roughness increased further to R_{rms} = 3.6 nm for 20 mins and R_{rms} = 4.3 nm for 40 mins deposition times.

Surface morphology for ZnO films grown on c-plane sapphire substrates as shown in Fig. 4.14 differ with r-plane sapphire substrates both in surface roughness and film structure. At the onset of growth as depicted in the 5

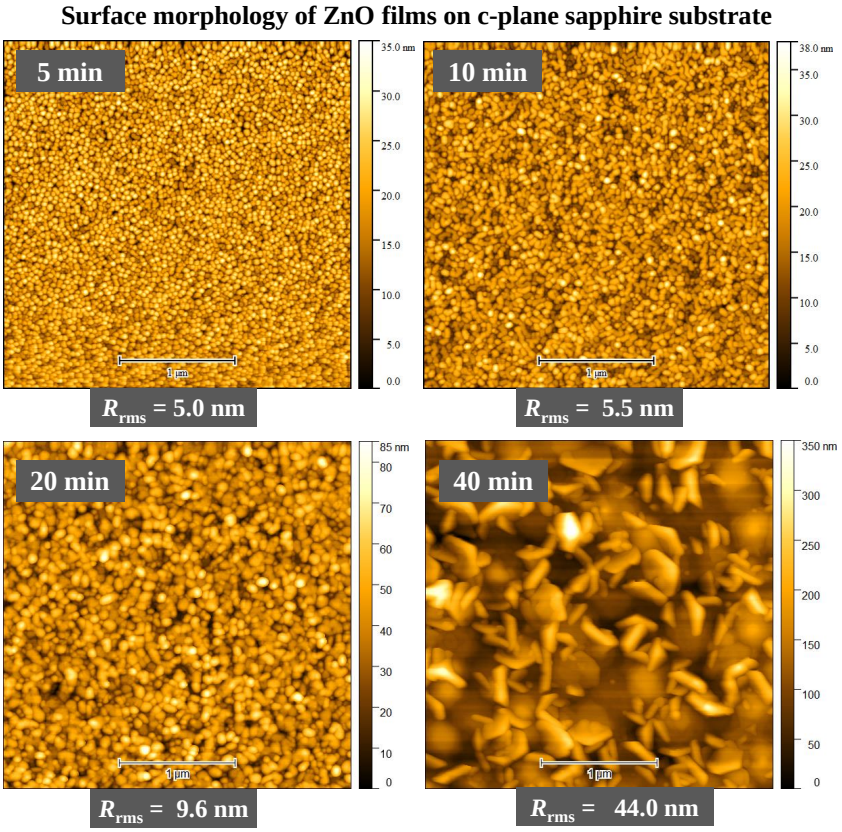


FIGURE 4.14: Surface morphology of ZnO film samples deposited at growth temperature of 500°C with 0.1 mol/L precursor on c-plane sapphire substrates at different growth times.

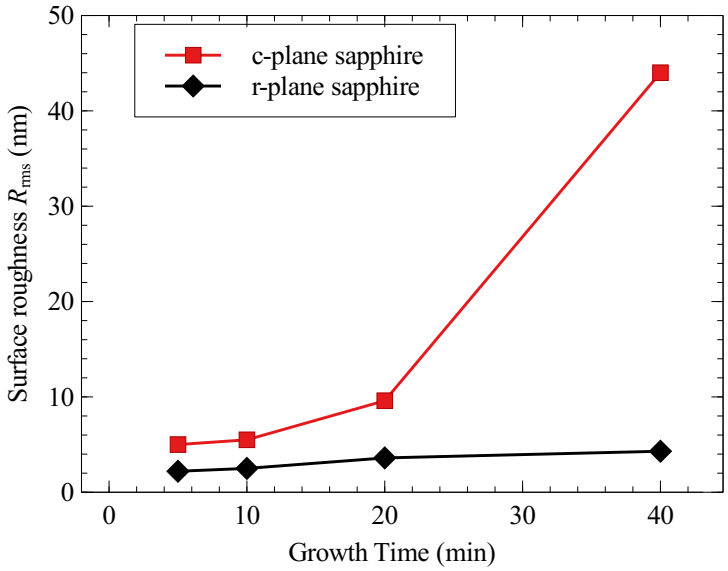


FIGURE 4.15: Variation in surface roughness with growth time for ZnO films grown on c-plane and r-plane sapphire substrates.

mins growth duration, dense and spherically shaped grains uniformly cover the surface of the substrate. These grains increased in size but unlike films on r-plane sapphire, are still isolated from each other as the growth duration and film thickness increases. With further increase in growth time and thickness, the film topography evolved from having dense isolated grains to having unique shape of nanostructure as shown for a 40 growth sample. Surface roughness for ZnO films grown on c-plane sapphire is R_{rms} = 5.0 nm for a 5 mins growth which increases to R_{rms} = 44 nm for sample grown for 40 mins. A comparison in the surface roughness of ZnO films deposited on c-plane and r-plane sapphire substrates at different growth times is shown in Fig. 4.15.

In addition to not having any amalgamation of grains elongated in a given direction, surface roughness for films on c-plane sapphire substrates is substantially different from r-plane substrate, with films generally smoother on r-plane substrate. There are only a few articles that compare morphological properties of ZnO films deposited on different crystallographic orientations of sapphire substrate. Interestingly, improved morphological smoothness of ZnO films deposited on r-plane sapphire is similar to the results obtained by Lee *et al.* [128]. In the report, atomic layer epitaxy was used to deposit 375 nm thick ZnO film on r-plane and c-plane sapphire substrates. Assessment of roughness showed that R_{rms} = 12.36 nm for ZnO film on r-plane sapphire substrate and R_{rms} = 30.94 nm for film grown on c-plane substrate. The variation in roughness may be associated with difference in surface energy. For growth on c-plane sapphire substrate, the polar nature of ZnO terminated by the basal plane of opposite charges has a net dipole moment which causes the surface energy to diverge [69, 128]. Thus the non-polar r-plane and m-plane ZnO film have a lower surface energy compared to the basal c-plane oriented films. This results in columnar morphology with relatively increased roughness for films grown on c-plane sapphire substrate [69].

4.6.4 Growth on amorphous quartz substrate

Growth of ZnO film was also performed on an amorphous quartz substrate at a deposition temperature of 500°C. The AFM micrograph of the surface of the ZnO film with a thickness of 120 nm deposited on quartz substrate is shown in Fig. 4.16. Film roughness with R_{rms} = 13.8 nm was significantly higher for the growth on quartz substrate relative to a film grown on the

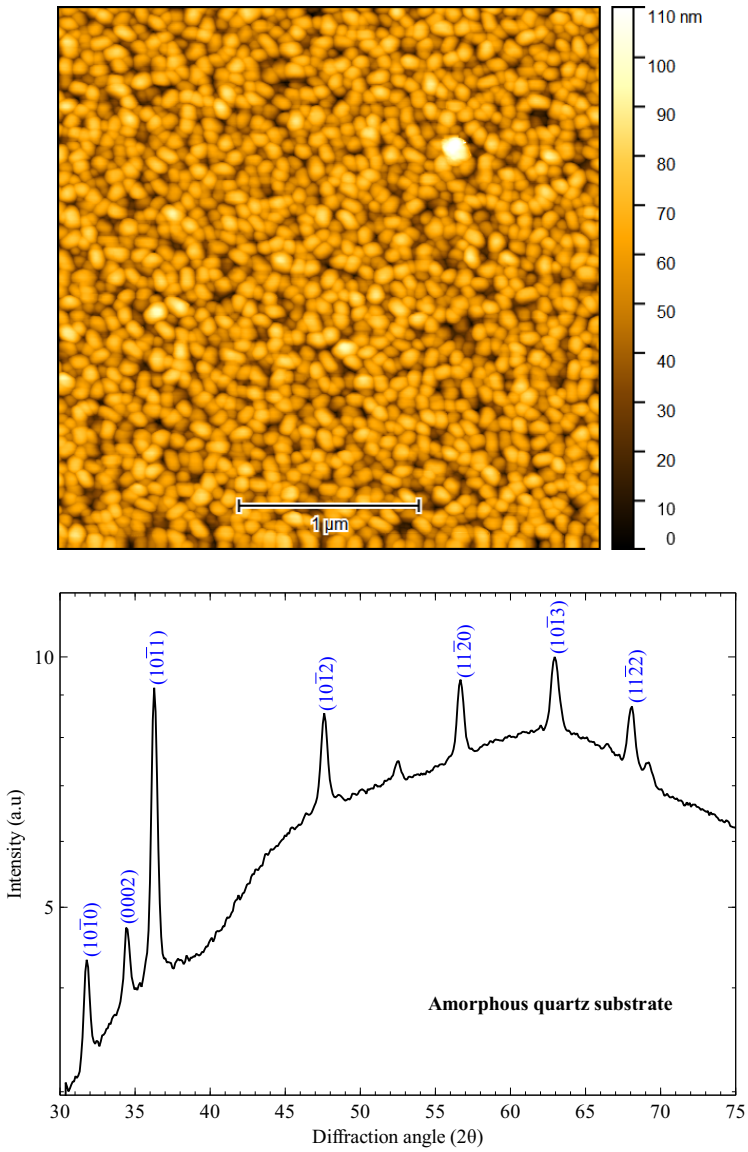


FIGURE 4.16: Surface morphology of ZnO film sample grown on amorphous quartz with its XRD pattern showing the presence of amorphous and crystalline compositions in the film.

r-plane sapphire of comparable thickness. The grains on the film are distinct and well defined with average grain size calculated to be 49 nm using the delineation by threshold approach available with the Gwyddion software analyses [73].

XRD analyses show the film to be polycrystalline in texture, depicted as several distinct diffraction peaks from different lattice planes. These multiple growth orientations of ZnO film are superimposed on a broad diffraction peak most likely originating from the amorphous quartz. In contrast to sapphire substrates, the surface of an amorphous quartz substrate does not

provide nucleation template for the preferential orientation of thin film during growth, hence no epitaxial relationship exists between the substrate and deposited film.

4.6.5 Film Uniformity

Among the reported limitations of other cost-effective growth techniques such as spin coating and spray pyrolysis is the non-uniformity of films deposited with these methods. Film porosity and non-uniformity often limit its use in device fabrication. In the case of spray pyrolysis, the droplet produced is much larger by a factor of 10 - 1000 than that produced in the mist-CVD process. Hence improved film uniformity can be obtained from the mist CVD technique [97] compared to spray pyrolysis. During growth, the precursor molecules in the aerosol diffuse to the heated substrate where they are adsorbed and consumed across a boundary layer. Film uniformity is dependent on the local diffusion flux to the surface.

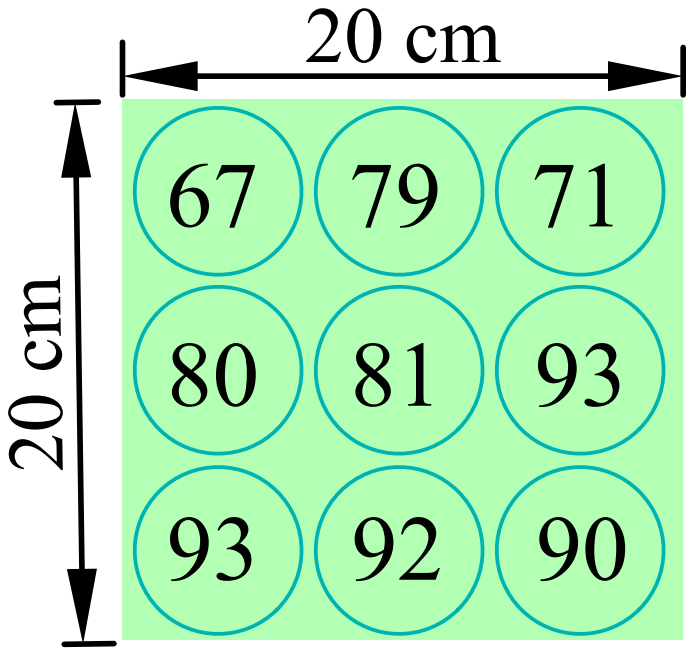


FIGURE 4.17: Variation of thickness across a 20 cm × 20 cm ZnO film deposited on Quartz substrate. The numbers represent thickness in nm.

Investigation of the homogeneity in film thickness was done by measuring the transmission on a circular 5 mm diameter region at various positions across ZnO film deposited on a 20 cm × 20 cm amorphous quartz substrate.

TABLE 4.2: Electrical properties of as grown ZnO film samples measured from room temperature Hall effect.

Temperature (°C)	Film thickness ±5 (nm)	Charge concentration n (cm^{-3})	Hall mobility μ_H ±1 ($cm^2/V.s$)	Resistivity ρ (Ω-cm)
300	120	1.1×10^{18}	4	1.3
350	75	1.8×10^{19}	9	2.4×10^{-2}
400	50	1.9×10^{19}	13	2.1×10^{-2}
450	48	1.1×10^{19}	11	6.7×10^{-2}
500	74	8.0×10^{18}	16	4.2×10^{-2}
550	93	1.3×10^{18}	16	7.6×10^{-1}

The variation in thickness was estimated by measuring the transmission at each position across the film surface, which was used to find the thickness based on the absorption coefficient found for other film samples where thicknesses were determined from etching and profiling of a step edge.

Fig. 4.17 indicates that film thickness becomes thinner further down in the direction of mist flow. The mean thickness across the 20 cm × 20 cm area shown in the figure is 83 nm with an average deviation of about 10%. Improvement in uniformity is usually achieved by increasing the flow rate of the carrier/dilution gas. The combined gas flow rate was set to 10 liters/min, optimized for the routine growth on a 10 cm × 10 cm sapphire substrate where deviation from the mean thickness is about 5 - 6 %.

4.6.6 Electrical properties

Hall effect measurement described in section 3.3.3 was used to investigate the electrical characteristics of the ZnO films. The electrical properties of as-grown ZnO films deposited on r-plane sapphire substrates indicate that films exhibit properties of an n-type semiconductor. Factors such as film thickness, deposition temperature and annealing were found to affect the electrical properties of deposited films.

The results in Table 4.2 indicate how charge carrier concentration n, mobility μ_H and resistivity ρ are influenced by the growth temperature. For the same reason explained previously relating to ZnO film sample grown at 300°C, mobility was the lowest at $4cm^2/V.s$ and resistivity was maximum (1.3 Ω-cm), despite having higher thickness than other samples shown in the table.

It can be observed that the electrical properties of film samples grown immediately above the decomposition temperature of zinc acetate (∼315°C) changed with improvement in n, μ_H and ρ. There is a dramatic reduction

in the resistivity of the films grown at 350°C, 400°C and 450°C when compared with sample deposited at 300°C. Charge carrier mobility also showed a trend of increase with deposition temperature. The increase in carrier mobility may be associated with the increase in grain size as the growth temperature increases. The effect of thickness on the electrical properties of ZnO film

TABLE 4.3: Electrical properties of ZnO films with different thickness.

Film thickness (nm)	Charge concentration n (cm^{-3})	Hall mobility μ_H ± 1 ($cm^2/V.s$)	Resistivityρ (Ω-cm)
43	6×10^{17}	8	1.5
85	3.1×10^{18}	9	2.0×10^{-1}
105	4.6×10^{18}	15	8.1×10^{-2}
204	1.7×10^{19}	22	1.6×10^{-2}
260	1.2×10^{19}	29	1.5×10^{-2}
380	1.4×10^{19}	32	1.4×10^{-2}
500	1.1×10^{19}	30	1.2×10^{-2}

is shown in table 4.3. All of the samples were grown at a standard growth temperature of 500°C with a precursor concentration of 0.05 mol/L. There is an observable trend between film thickness and all of the electrical assessment metrics. The charge carrier concentration and mobility increase as the thickness of the film increases while resistivity reduces with film thickness. The mobility increases from 8 $cm^2/V.s$ for a 43 nm film to about 32 $cm^2/V.s$ for a 380 nm thick film. The increased mobility with thickness can be explained by the formation of larger grain sizes which become more compact with thickness increase [53]. Also, improved film conductivity with increase in thickness is associated with the reduction in grain boundaries due to increase in size of the grains. As observed in table 4.2, charge carrier concentration reduced from 1.8 $\times10^{19}\,cm^{-3}$ at 350°C to 8.0 $\times10^{18}\,cm^{-3}$ at 500°C for film samples of similar thickness. The observed reduction in carrier concentration is due to rearrangement of growth species at increased growth temperature leading to reduction in crystal defects. Similarly the carrier concentration increases with film thickness due to higher concentration of these defects acting as donors.

The trend in resistivity as a function of film thickness is shown in Fig. 4.18. The plot shows a decreasing trend in resistivity as thickness increases. Similar to an explanation for the increase in mobility with thickness already discussed, such a trend in film resistivity is due to larger grain sizes leading to a reduction in grain boundaries and an increase in charge carrier mobility.

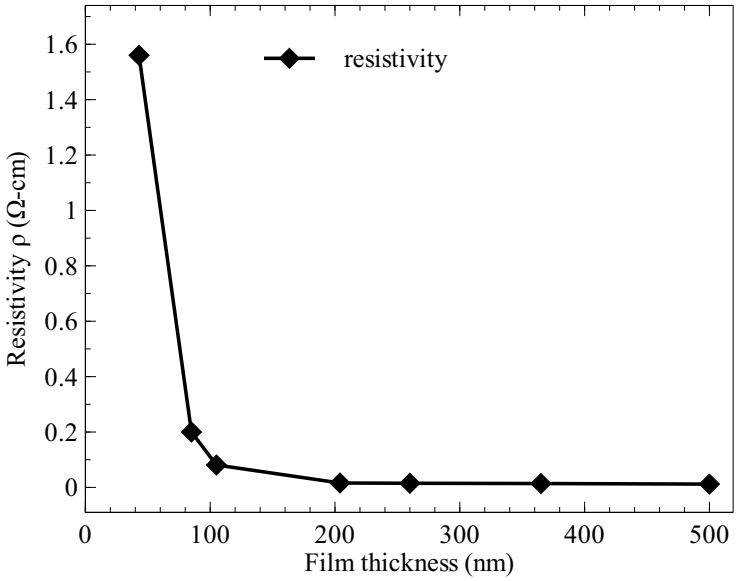


FIGURE 4.18: Variation of resistivity for ZnO films deposited at 500°C on an r-plane sapphire substrate.

The very low resistive ZnO films of $\approx 10^{-2}$ Ω-cm indicates an interesting capability of mist-CVD growth technique for achieving a highly transparent and well-conducting film for TCO application. Such a resistivity value is noteworthy for an undoped ZnO film compared to several other growth techniques. The most likely source of donor atoms that results in such a low resistivity value for unintentionally doped ZnO film is Al. The fine channel reactor as described in Chapter 3 is made of aluminum metal which has a low melting point of about 630°C. Aluminum atoms acting as donors most likely diffuse into the crystal lattice during film growth. Additionally, Al donor atoms can also originate from the sapphire substrate used for growth. Optical studies from PL spectroscopy presented in chapter 5 confirm the incorporation of Al donor atoms in the crystal lattice of our films.

Another interesting result from electrical characterization shows the very low resistive film samples deposited at temperatures between 350°C - 450°C. These results indicate that highly conductive films can be achieved at relatively low growth temperature for TCO application by using zinc acetate as precursor material and performing growth at a temperature just above its thermo-gravimetric decomposition point of 315°C. The relatively higher resistivity value of 1.5 $\Omega-$cm found for a film sample with a thickness of 43 nm is associated with an increase in the strain on film caused by the lattice mismatch between film and the substrate. Ghosh *et al*, [67] reported a strain-induced exponential increase in the resistivity in ZnO films. With higher

strain for a very thin film, there is a higher density of grain boundaries associated with small grain size and this tends to reduce carrier mobility and increase the resistivity of the film.

4.6.7 Effects of thermal Annealing

An investigation was carried out to understand the effects of thermal annealing on the electrical properties of ZnO film. A sample of ZnO film with a thickness of 260 nm deposited at 500°C was annealed under a O_2 gas atmosphere successively at 600°C, 700°C and 800°C each for a duration of 30 minutes. Thermal annealing is used as an effective means of improving the crystalline quality of films. The electrical properties of as-grown and annealed

TABLE 4.4: Effect of annealing on the electrical properties of ZnO film sample

	Charge concentration n (cm^{-3})	Hall mobility μ_H ± 1 ($cm^2/V.s$)	Resistivityρ (Ω-cm)
As grown	2.0×10^{19}	31	1.0×10^{-2}
Annealed 600°C	1.4×10^{18}	36	1.2×10^{-1}
Annealed 700°C	6.7×10^{17}	26	3.6×10^{-1}
Annealed 800°C	6.2×10^{17}	25	4.0×10^{-1}

film sample are represented in Table 4.4. The effect of annealing at 600°C is an improvement in the carrier mobility and reduction in the conductivity of the film. The carrier mobility which was found to increase at an annealing temperature of 600°C, however decreased with further annealing at 700°C and 800°C. Under an oxygen rich ambience, the conductivity and charge carrier concentration of the film monotonically decreased for each successive annealing step. Annealing in oxygen atmosphere allows for the thermally assisted diffusion of oxygen atoms in the lattice to reduce oxygen vacancies, a well reported origin of n-type conductivity in ZnO. The result of thermal annealing in O_2 shows that electrical conductivity of mist-CVD grown film can be controlled to a desirable state through an annealing process. For instance, the conductivity of film can be reduced with carrier concentration reduction from $\sim 10^{19}$ cm^{-3} to $\sim 10^{17}$ cm^{-3} suitable charge carrier concentration for fabricating Schottky contacts and transistors. The Hall mobility improved for the first annealing step increasing from 31 to 36 $cm^2/V.s$ after

annealing at 600°C. However, a subsequent annealing step caused a reduction in the mobility which may be a result of thermal damage caused by high temperature or longer annealing time.

4.7 Summary

In the mist-CVD growth of ZnO, the use of aqueous ammonia as precursor solvent instead of organic solvents enables a safer and less volatile growth recipe for film nucleation.

Aqueous ammonia has two key functions - helps to improve atomization of liquid precursor in contrast to water only. Additionally, it provides a basic pH environment for ZnO crystallization through growth intermediates.

Polar ZnO with c-axis (0001) crystal orientation was deposited on a c-plane sapphire substrate while ZnO films with a-plane($11\bar{2}0$) crystalline orientation were obtained on r-plane sapphire substrates. Film crystal quality measured through rocking curve XRD analysis on ZnO grown on r-plane sapphire indicated crystalline improvement as growth temperature increases.

ZnO films deposited on r-plane sapphire substrates showed smoother surface topography compared with films deposited on c-plane sapphire. Crystallite sizes increase at the thickness of deposited film increases. As film thickness increases, elongation of grains oriented in a given direction leading to surface anisotropy is noticed in films deposited on r-plane sapphire.

Electrical properties of ZnO films grown on r-plane sapphire substrates measured through Hall effect analyses show increase in carrier mobility, charge concentration and conductivity with increase in film thickness. Annealing in oxygen gas reduced the charge concentration and increased resistivity.

Chapter 5

Optical Properties of Mist-CVD Grown ZnO

5.1 Introduction

Some of the very important properties of ZnO such as its direct bandgap and high exciton binding energy continue to inspire interest in it as a semiconductor of choice in a range of applications. These properties have promising potential applications in optoelectronics such as in UV light-emitting diodes and laser diodes among others. Compared to the technical merit achieved by the development of GaN-based UV LEDs, ZnO gains a more favorable interest for developing UV LEDs considering that its exciton binding energy is about 60 meV compared to GaN which is 25 meV. Additionally, ZnO is radiation hard with good thermal resistance making it particularly useful as transparent contacts in solar cells. Further, ZnO powders, films and ceramics have found recent applications in scintillation applications.

This chapter focusses on the optical properties of mist-CVD deposited ZnO films studied through light absorption/transmission and photoluminescence. Description of the experimental setup for these optical characterization measurements is outlined in section 3.3.2.

5.2 Transmission/Absorption

This section discusses the results of transmission spectroscopy done on some selected ZnO film samples. Experimental measurements were performed at room temperature in addition to liquid helium temperature. A discussion on the results of optical studies on ZnO films done through transmission and photoluminescence spectroscopy is presented .

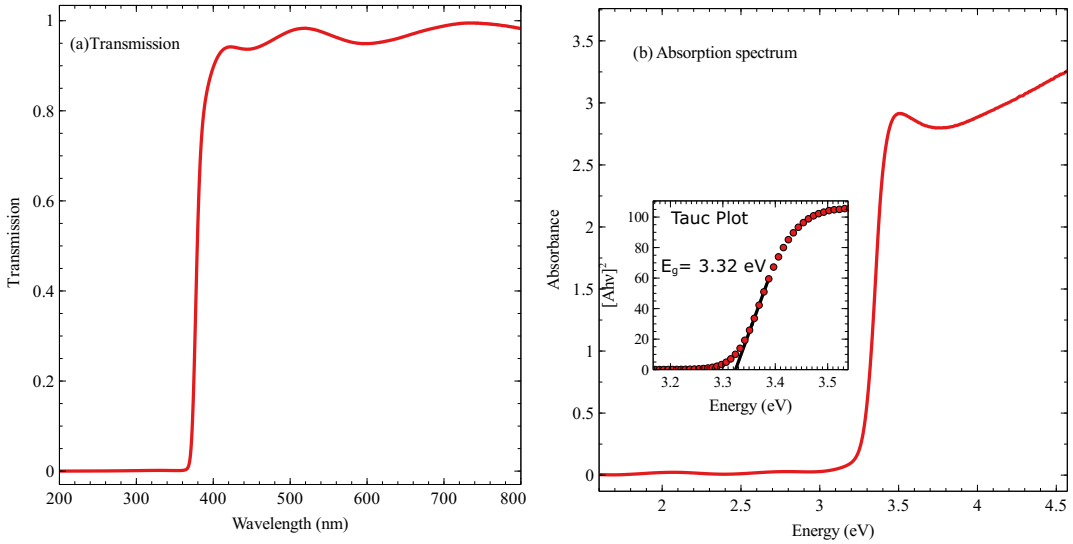


FIGURE 5.1: (a) Room-temperature optical transmission as a function of incident photon wavelength for a 380 nm thick ZnO film deposited on an r-plane sapphire substrate. (b) Absorbance spectrum plotted on the energy axis. Inset - A Tauc plot used to determine the optical bandgap of the film.

5.2.1 Room Temperature Transmission

Qualitative visual assessment of the ZnO films indicates that ZnO films deposited through the mist-CVD process have a clear optical appearance with a smooth specular surface over the whole substrate. Fig. 5.1 shows room temperature transmission and absorption spectra for a 380 nm thick ZnO film deposited on sapphire substrate by the mist-CVD growth technique at a substrate temperature of 500°C. It can be observed from the plots that the ZnO film is highly transparent for most of the visible region with an abrupt transition to light absorption commencing at a wavelength of about 370 nm. The uniform transmission spectrum indicates that optical transmission is not degraded by light scattering from rough surface morphology or inhomogeneous material. The absorption curve shows that the deposited ZnO film exhibited the typical characteristics expected of ZnO material with strong photon absorption at photon energy above its bandgap energy. An interference fringe pattern is observed in the visible region of the transmission spectrum due to the interaction of incident photons as it passes through the air-film-substrate interface. The bandgap energy found for a 380 nm ZnO film using the Tauc plot shown on the inset of Fig. 5.1(b) is 3.32 eV.

The plot in Fig. 5.2 shows the transmission spectra of ZnO films of varying thickness deposited on an r-plane sapphire substrate. It is observed that

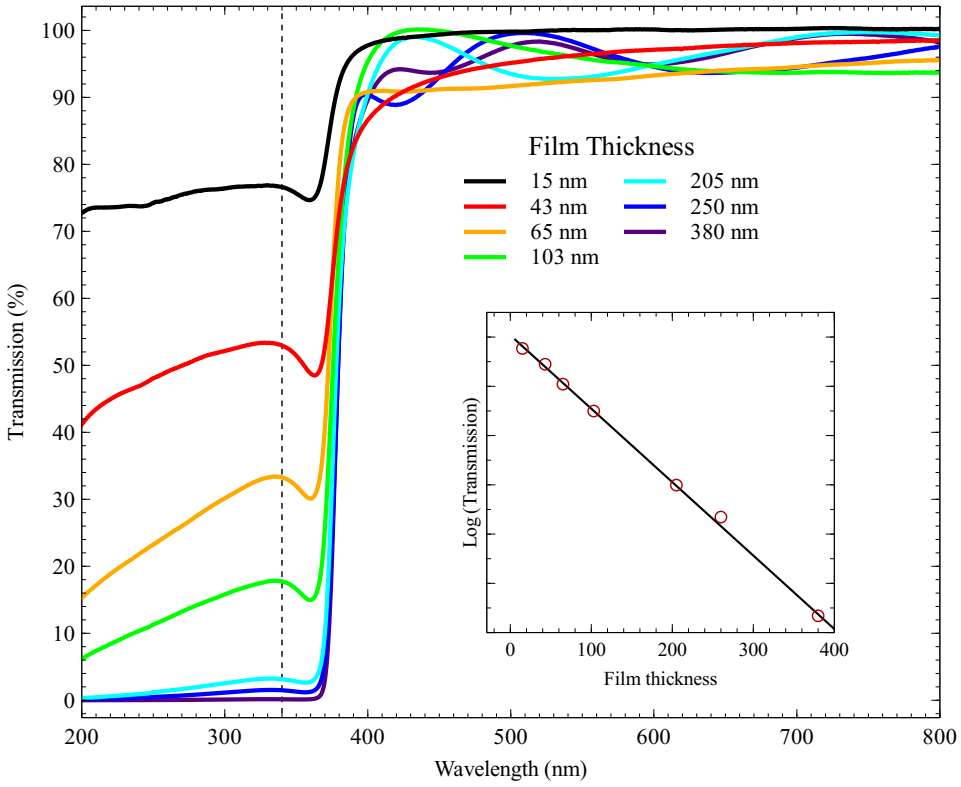


FIGURE 5.2: Transmission spectra of ZnO films of various thickness. Inset - a plot of logarithm of transmission against film thickness measured after etching with a linear relation that confirms an exponential relationship between film thickness and photon absorption.

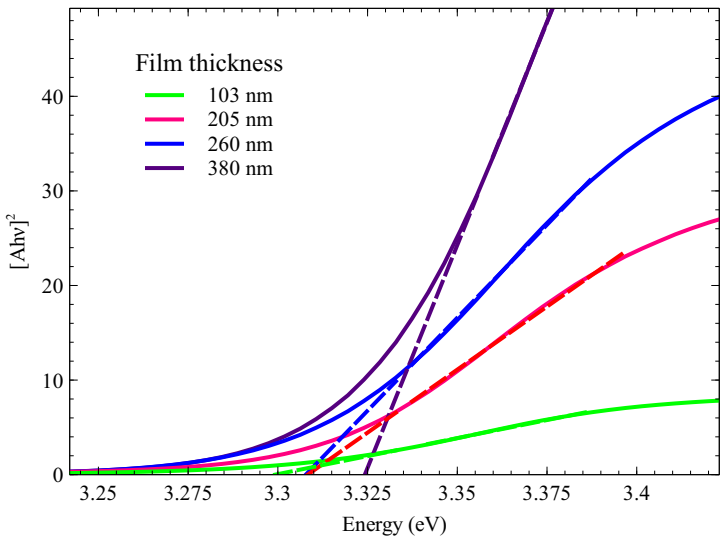


FIGURE 5.3: Tauc plot for some selected ZnO films with varying thickness showing slight variation in the extrapolated bandgap energy.

the absorption edges in the transmission spectra for the films slightly shifted to longer wavelength as the film thickness increases. This shift in the absorption edge is noticeable for the 15 nm thick film relative to other samples. The shift in the absorption edge is attributed to the presence of micro-strain and dislocations which tend to relax as the film thickness increases [65].

The indicated dashed line corresponds to transmission at an incident photon wavelength of 340 nm. The logarithm of transmission at 340 nm for the samples is plotted on the inset figure. The choice of transmission data at 340 nm is to enable quantitative comparison to be made on the samples right after photon absorption near the absorption edge and avoid noisy data at lower wavelengths. The linear fit to the data confirms the exponential relationship between film thickness and light absorption/transmission. This follows from the Beer-Lambert's law which gives an exponential relationship between transmitted light through a material and the thickness of the material.

The bandgap found for our films varies slightly with increasing film thickness as shown in Fig. 5.3. The bandgap energy was found to be 3.29 eV, 3.30 eV and 3.31 eV for films with a thickness of 103nm, 205 nm, and 260 nm respectively. This range of bandgap energies is slightly higher than typical bandgap values of 3.28 - 3.29 eV reported for high-quality undoped ZnO films where the Tauc method was to evaluate bandgap [216, 164]. The most likely explanation for a slightly increased bandgap as the thickness increases is the Burstein-Moss effect. This effect explains the widening of the bandgap due to some energy states close to the conduction band being filled as a result of increased electron carrier concentration. An increase in film thickness corresponds to larger grain sizes, less strain, and higher film conductivity. The blue shift in bandgap is in agreement with electrical measurements from Hall effect performed for these samples which confirmed that charge carrier concentration moderately increased as film thickness increases.

Even though the extracted bandgap energy for a 380 nm film sample was found to be $\sim$3.32 eV, that is still lower than the 3.37 eV reported for bulk ZnO material at room temperature [114]. Earlier reports have erroneously attributed the redshift of the bandgap derived from the Tauc plot with respect to bulk ZnO to effects of strain on the film [204]. However, it is now accepted that the discrepancy is linked to extrapolation and interpretation of the Tauc plot method for finding the bandgap [164, 183]. The Tauc plot is based on the assumption that optical absorption is a simple phenomenon and relies solely on the extrapolation of the main absorption edge due to

electronic transitions between the valence and conduction bands. However, there exist some other exciton related optical processes close to the absorption edge in ZnO films which may only be resolved in films of high quality and/or sufficient thickness. Because the Tauc plot method may not account for these additional exciton related transitions, the value of the bandgap may appear to be lower than the bulk. By accounting for the exciton binding energy of 60 meV when calculating the bandgap energy, the extracted bandgap increases from 3.32 eV to 3.38 eV which is closer to that of the bulk. Further, while the Tauc method provides a handy technique to estimate the bandgap from the transmission spectrum in thin films, there may be additional issues with the accuracy of fit due to effects from lower energy sub-gap absorption usually called the "Urbach tail" effect [220, 34].

5.2.2 Temperature Dependent Transmission

By studying the effect of temperature on the optical properties of a semiconductor, important information such as excitonic effects and electron-phonon interaction can be derived. Investigation on the temperature dependence of the bandgap is important because of certain reasons. One is that it enables the understanding of the fundamental factors that contribute to the bandgap shift with temperature. It also enables one to understand the practical capabilities for semiconductor devices when operated over a wide range of temperatures.

The experimental setup for the temperature-dependent transmission measurement is similar for that of room temperature except that the sample is attached over a hole on a copper cold finger using a silver paste on the edges of the sample. This enabled temperature control while still allowing an optical path through the sample. A reference sample, a bare sapphire substrate was attached to the second hole on the cold finger and was used for baseline correction. A turbopump was used to evacuate the cryostat up to a pressure of 10^{-5} Torr which prevented condensation on the cryostat window. A cryopump with closed cycle helium refrigerator cooled the sample while a heater attached to the cold finger was used to maintain the desired temperature ranging from 10 K to room temperature. A mounted rail enabled the cryostat containing the sample to be moved into the beam path of the spectrophotometer system.

For measurements, the sample was first cooled to 9K and transmission data were acquired at various set temperatures while heated back to room

temperature. Before transmission measurement at each set temperature, a waiting period of about 5 minutes was kept to ensure that both the sample and the cold finger were in thermal equilibrium. The contribution to the spectral response of the film by the sapphire substrate was removed from the actual transmission data via the reference sample attached to the cold finger. It was found that a bare sapphire substrate used for baseline correction only has a small reduction in transmission with almost no spectral response with temperature.

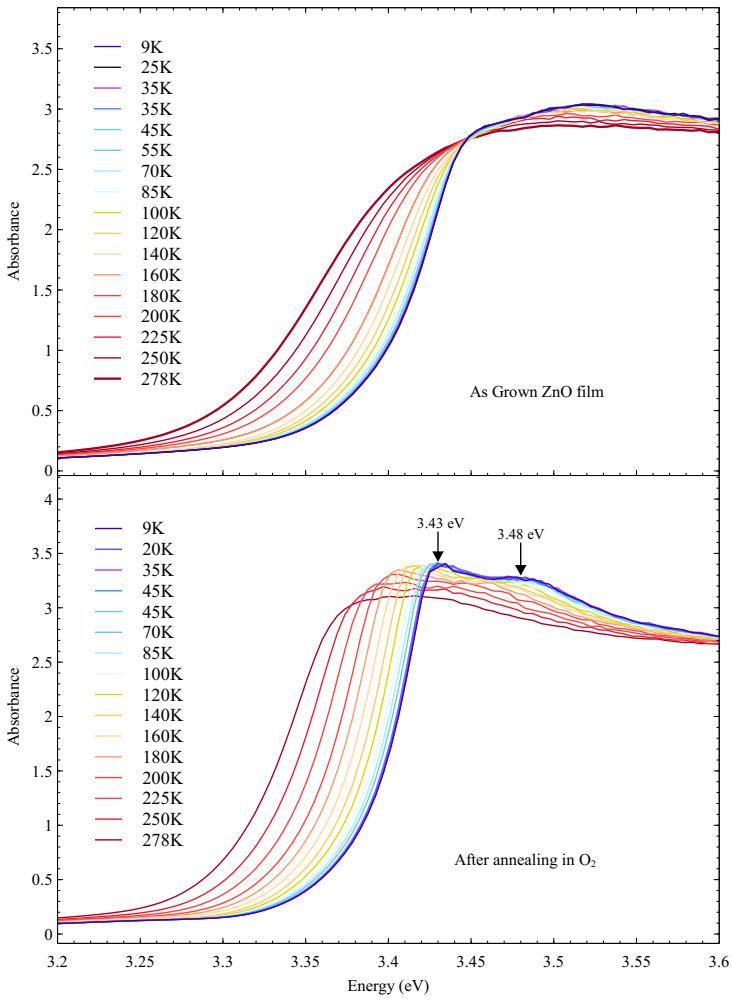


FIGURE 5.4: Temperature dependent absorption spectra for ZnO film at a temperature between 9 - 275 K. Spectra acquired before and after annealing with sample placed in a cryostat and cooled down with a cryopump.

Fig. 5.4 shows the temperature-dependent absorbance spectra for ZnO film with a thickness of 380 nm before and after annealing at 800°C. Annealing of the film sample was done first in O_2 atmosphere at 600°C followed by

further successive annealing at 700°C and 800°C each for 30 minutes duration (electrical measurements were done for each annealing step). It can be observed that as the crystal temperature during transmission measurement increases, the fundamental absorption edge is red-shifted to longer wavelengths. A Tauc plot at different temperatures used to find the temperature-dependent optical bandgap of as-grown ZnO film sample is shown in Fig. 5.5. An increase in temperature causes the vibrational energy in atoms to increase leading to a greater interatomic distance. The more adjacent atoms move further away, the less the periodic potential felt by an atom which leads to a decrease in potential energy of the electron. The electron's potential energy is one factor that determines the band characteristics of a semiconductor with decreased potential energy corresponding to reduced bandgap energy.

It can be seen that annealing enhanced excitonic related peaks in the absorbance spectra acquired at low temperatures. Muth *et al.* [159] had reported these peaks and wrongly assigned them to the A and B excitons which brought some debates on such an assignment. The first peak centered at 3.43 eV is a combination of A and B excitons while the position of the second peak at $\approx$ 3.48 eV is closely indicative of a C-exciton based on the energy splitting of approximately 49 meV between A-C excitons. The enhancement of excitonic peaks after annealing shows improvement in the crystalline quality of film post-annealing. The inset in Fig. 5.5 shows that bandgap decreases across all crystal temperatures after annealing the sample. The reduction in charge carrier concentration n by the annealing process is considered to be the reason for the decrease in the energy bandgap post-annealing. This observation can be explained based on the Burstein-Moss shift where reduction in n due to annealing leads to a decrease in bandgap energy, since fewer electrons occupy energy states above the conduction band minimum. For this film sample, Hall measurement showed that as-grown n was $\sim 10^{19}$ cm^{-3} but reduced to 6.2×10^{17} post-annealing.

Some empirical and semi-empirical models have been proposed that quantify temperature-dependent shifts in the bandgap energies of semiconductors. One of the empirical and commonly applied models is the Varshni equation [222] which gives a non-linear relationship between bandgap energy dependence and temperature.

$$E_g(T) = E_g(0) - \frac{AT^2}{T+B} \tag{5.1}$$

where A and B are fitting parameters specific to a particular semiconductor

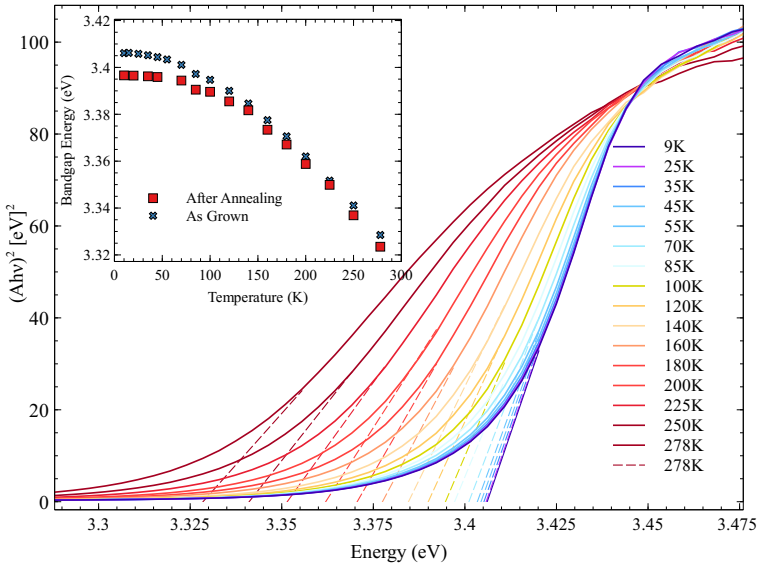


FIGURE 5.5: Temperature dependent Tauc plot derived from transmission data of as-grown ZnO film sample. Extrapolation of the linear region was used to find the bandgap at a given temperature. Inset - Bangap energy dependence before and after annealing.

and $E_g(0)$ is the bandgap energy at 0 K. The Varshni relation is known to fit well with various group II-VI semiconductors such as ZnO, however, the physical meaning of parameter B is not explained even though it may be related to the Debye temperature in some semiconductors [196]. The Varshni model fit for the temperature dependent bandgap is shown in Fig. 5.6(a) which gives the A and B fit coefficients as 8.5×10^{-4} eV/K and 817 K respectively. The parameter A is close to the value of 8.2×10^{-4} eV/K reported for bulk ZnO [20]. The fitting quantity B has previously been given as 672 K [20], 660 K [171] and 700 K [229]. A value of B = 817 K returned the best fit for this sample and $E_g(0)$ is derived to be 3.407 eV. The fit coefficients are close and in agreement with the values obtained by other reported works that fitted the model to temperature dependent shift in bandgap energy for ZnO. Using this model, Granerod *et al.* [70] obtained B and A coefficients as 338 K and 3.8×10^{-4} eV/K respectively.

An alternative model that describes bandgap energy dependence with temperature is the Manoogian-Wolley equation. Unlike the Varshni equation, model parameters derived from Manoogian-Woolley equation have more

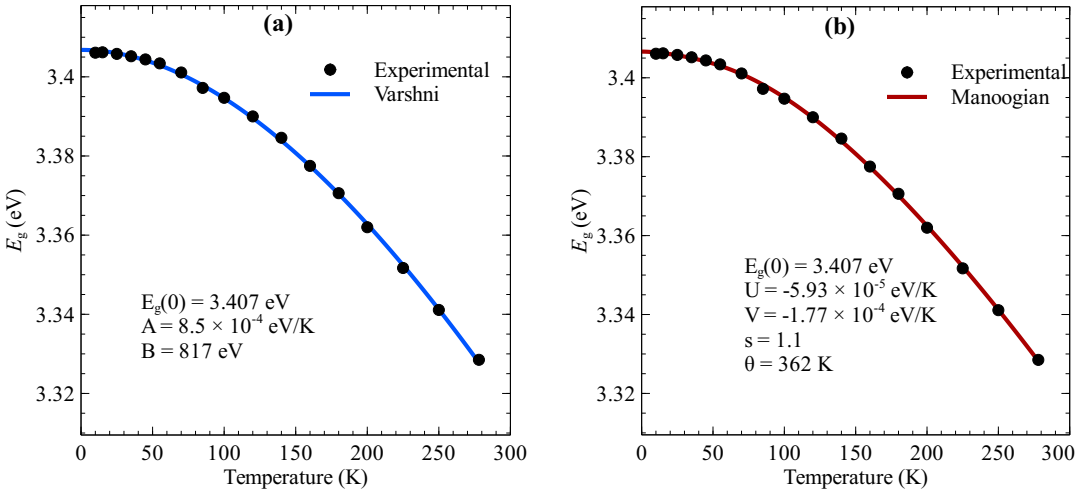


FIGURE 5.6: Fitting to temperature dependent bandgap shift using (a)Vershni and (b) Manoogian models.

physical relevance to the fitted experimental data. Manoogian-Wolley equation is expressed as:

$$E_g(T) = E_g(0) + UT^s + V\theta(\coth(\theta/2T) - 1) \tag{5.2}$$

where $E_g(0)$ is the bandgap at 0 K. The model improves the Bose-Einstein model [179] by accounting for the semiconductor's crystal lattice dilation dependence with temperature through an additional term UT^s in the equation while $V\theta[\coth(\theta/2T) - 1]$ accounts for the contribution of electron phonon interaction [124]. The coefficients obtained by fitting the Manoogian-Wolley model on the experimental data is comparable to the reported article by Hamby *et al.* [75] with values $E_g(0)$ = 3.379 eV, U = -5.04 $\times 10^{-5}$ eV/K, s = 1.01, V = -1.84 $\times 10^{-4}$ eV/K and θ = 398.4 obtained by fitting Manoogian-Wolley model to temperature dependent bandgap shift on bulk ZnO.

Comparing our results with other published works in academic literature shows that the optical bandgap determined from transmission measurement and fitting of the above models seem slightly higher than $\approx$ 3.38 eV [30] mostly reported for ZnO films at very low temperature (< 10 K). Hall electrical measurement for this sample indicates that the charge carrier concentration is 1.4 $\times 10^{19}$ cm^{-3} suggesting that unintentional shallow donor impurities are incorporated in the ZnO films. Due to the higher concentration of donor atoms, some energy states above the conduction band become occupied such that inter-band optical transition from photon absorption results in a blue-shifted absorption edge and an increase in the bandgap of ZnO. This apparent increase in bandgap of a semiconductor caused by higher carrier

concentration is termed the Burstein-Moss shift.

5.3 Bandgap Engineering - Mg doped ZnO

A possible way at which the bandgap of ZnO can be altered is by doping with group II elements, which can create impurity states and shift the Fermi level [5]. Since Mg^{2+} ion radius of 0.57 Å, and Zn^{2+} ion radius of 0.60 Å are comparable, Mg serves as a suitable dopant that can replace Zn atom in the lattice. Besides, the higher bandgap energy of MgO of $\sim$ 7.4 eV enables widening of the bandgap in a $Mg_xZn_{1-x}O$ alloy. Therefore, varying the content of Mg in ZnO lattice provides a means to tune the bandgap to higher energy.

An investigation to determine whether Mg doping can successfully be done on mist-CVD grown ZnO films was carried out. Studies on magnesium doping were performed by adding magnesium acetate salt to a solution of zinc acetate before the growth of films. Growths of ZnO:Mg thin films with thicknesses about 210 nm were deposited at a growth temperature of 500°C on r-plane sapphire substrates at 5%, 10%, 20% and 40% fractional mass concentration of Mg in the precursor solution.

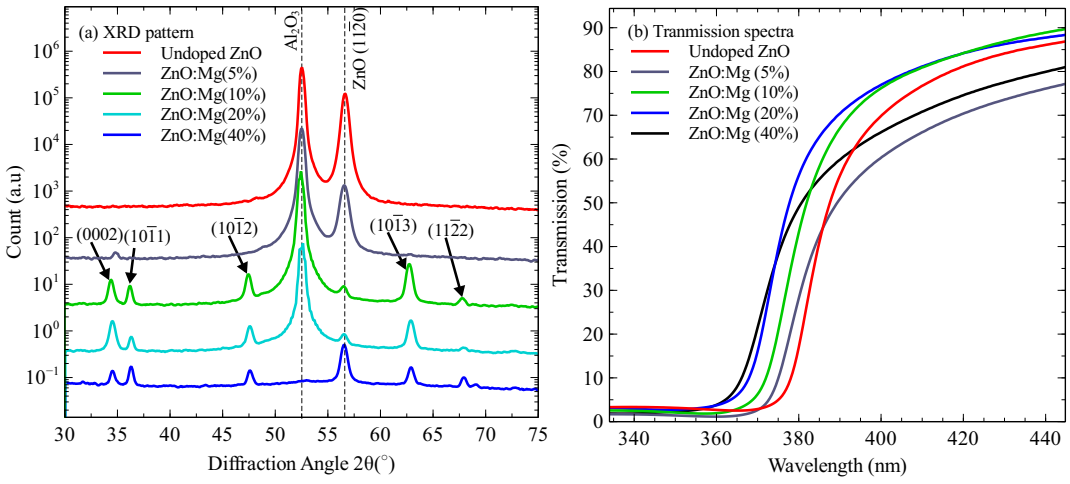


FIGURE 5.7: (a) XRD spectra (b) Transmission spectra for undoped ZnO and Mg-doped ZnO films

The diffraction pattern and transmission spectra for ZnO undoped film and ZnO:Mg samples deposited with varying fractional mass concentrations of magnesium acetate in the precursor solution are shown in Fig. 5.7. It is observed from the XRD pattern that magnesium incorporation in the film introduced multiple crystalline phases resulting in changes in the structural

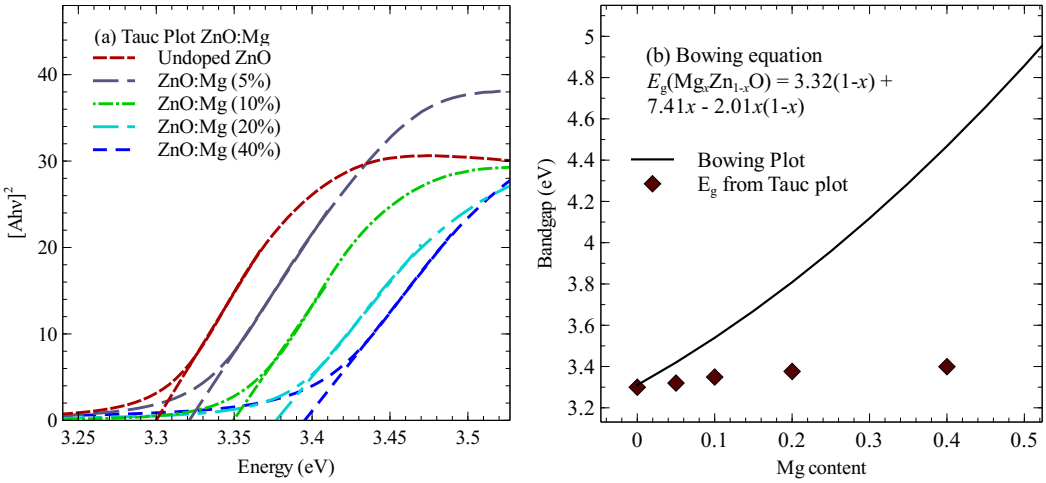


FIGURE 5.8: Tauc plot showing variation in bandgap energies with concentration of Mg (b) Bandgap energies compared with expected theoretical value based on Bowing equation.

properties of Mg-doped films. The slight shift in the 2θ angle for (0002) and $(10\bar{1}1)$ diffraction peaks with an increase in the fractional mass of Mg may be related to the distortion in the lattice structure of ZnO due to addition of Mg. It is of note that with Mg doping, the polycrystalline phases all originate from ZnO with no observable diffraction peak from MgO. This indicates that Mg segregation in the form of MgO did not occur as a result of the doping, and suggests that Zn atoms are more active than Mg and preferentially reacts with oxygen [86]. For the ZnO:Mg(40%), a sapphire peak is absent on the XRD pattern. This may be related to a relatively low signal strength with increased poly-crystallinity.

The transmission spectra indicate that the incorporation of Mg in the ZnO lattice results in a slight shift in the absorption edge as the doping concentration of Mg increases. The blueshift in the absorption edge corresponds to the widening of the bandgap energy with increased Mg concentration as illustrated in the Tauc plot of Fig. 5.8(a). It is seen that the bandgap energy increases from 3.30 eV for undoped ZnO to 3.39 eV for the ZnO:Mg(40%) film. This shift in bandgap energy suggests an upper limit of approximately 5% incorporation of Mg based on the bowing relation.

The bandgap energy gap of such a ternary compound is a function of the x concentration of Mg and is determined using the bowing equation [230].

$$E_g(\mathrm{Mg}_x\mathrm{Zn}_{1-x}O) = (1-x)E_g(\mathrm{ZnO}) + xE_g(\mathrm{MgO}) - bx(1-x) \tag{5.3}$$

where b is the bowing parameter that characterizes the deviation from linearity, $E_g(ZnO)$, $E_g(MgO)$ and $E_g(Mg_xZn_{1-x}O)$ are the bandgap energies of ZnO and MgO and MgZnO films. Using a bowing parameter b = 2.01 as reported by Ref. [230] and setting the bandgap energies of ZnO and MgO as 3.32 eV and 7.41 eV, a bowing plot for the ZnMgO is obtained. A plot of the theoretical bandgap variation according to the bowing equation and the experimental bandgap energies extracted from the Tauc plot at a varying concentration of magnesium is shown in Fig. 5.8.

It can be observed that incorporation of Mg in the ZnO lattice results to changes in both the optical and structural properties of doped films. However, since the widening of the bandgap energy is not consistent with the expected changes based on Eq. 5.3, it is most probable that incorporation of Mg in the ZnO lattice is minimal irrespective of the concentration, even for magnesium acetate making up to 40% fractional mass concentration in the precursor.

As has been described in Sec. 4.6.1, the growth rate and the number of growth species available for crystallization are dependent on the pH of the precursor solution. It is then most probable that the pH of the precursor solution is to be optimized separately for magnesium acetate and zinc acetate. However, only one solution chamber and an ultrasonic generation system is used for our research. A possible way of increasing the bandgap with Mg doping to closely follow the bowing relation in Eq. 5.3 is to introduce a separate precursor chamber for Mg and Zn constituent precursors while optimizing each with respect to pH. Atomized growth species from Mg and Zn precursors can, therefore, be mixed in the reactor chamber for film nucleation.

5.4 Photoluminescence Spectroscopy

Due to the desirable properties of ZnO such as its direct bandgap and exciton binding energy, it continues to gain research attention as a potential material for fabricating devices in the optoelectronic industry. With its wide direct bandgap, the expectation is for ZnO crystal to emit photons in the ultraviolet and UV region (366-388 nm). Photoluminescence (PL) spectroscopic technique is widely applied to study the luminescence properties of ZnO crystal and to identify impurities and defects. PL analyses thus provide a useful tool to study the potential applications of ZnO nanostructures in devices that involve light emissions such as light-emitting diodes and lasers. There are wide

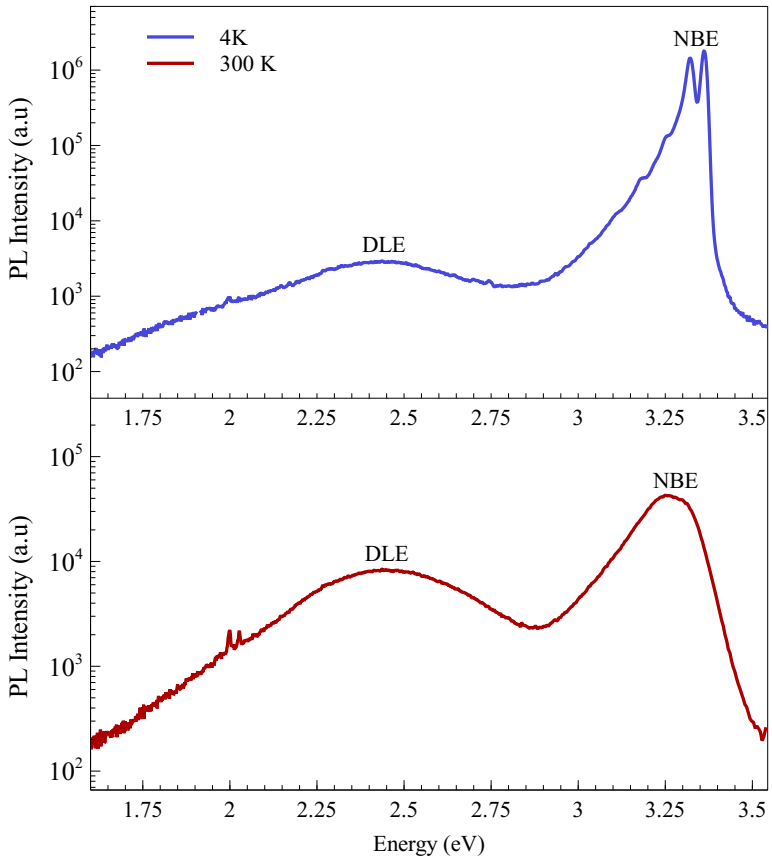


FIGURE 5.9: PL spectra for a 380 nm thick ZnO film sample acquired at room temperature (∼300 K) and a cryogenic temperature of 4K.

reports on various structures of ZnO including film, bulk crystals, nanowires, and other nanostructures which typically exhibit two luminescence bands - a narrow peak near the band edge (NBE) which is attributed to excitonic recombinations [149] and an additional broad deep-level emission (DLE) band in the visible region. The origin of the visible band is still debatable although it is most likely associated with defects in the crystal structure such as Zn interstitials and oxygen vacancies [44].

Fig 5.9 shows typical PL spectra acquired at room temperature and 4K for a 380 nm thick, as grown ZnO film deposited at 500°C on an r-plane sapphire substrate. Room-temperature PL spectra show that luminescence is dominated by NBE emission in the UV region ascribed to excitonic recombinations originating from a free exciton [95]. There are two distinct PL peaks observed in the NBE at 4K which are further discussed in the next section on temperature-dependent PL. Also observed is a broad emission band at lower energy attributed to the presence of native defects and crystal imperfections.

At room temperature, the NBE peak is centered is at 3.27 eV and a broad defect band emission peaked at approximately 2.44 eV. The ratio between the intensity of UV emission to the DLE is about 5 at room temperature and increases to about 620 at 4K. Further experiments to investigate the behavior and assignment of chemical origin to these PL features was done through a temperature-dependent PL measurement discussed next.

5.4.1 Temperature Dependent PL

At low cryogenic temperature, the PL emission of ZnO is dominated by bound excitons whereas, at a higher temperature, free excitons take over. The paper by Meyer *et al.* [149] provides a good reference for the identification of excitonic recombinations and their chemical identities, even though there are still some disputes on the origin and assignments of these recombinations lines.

PL spectra for a ZnO film sample with a thickness of 380 nm deposited on an r-plane sapphire substrate are shown in Fig. 5.10. For the 4K PL spectrum, there are clear and distinct recombinations lines originating from excitons bound to lattice defects. The emission at 3.362 eV can be assigned to neutral donor-bound exciton (D^0X). This recombination line typically labeled as I_6 at 3.3602 eV in the review paper of Meyer *et al.*, [149] is assigned to exciton bound to Al impurities acting as donors. This emission line is commonly seen in the PL spectroscopy of films deposited on Al_2O_3 substrates. The likely origin of Al impurity is the fine channel mist CVD reactor system which is fabricated with aluminum (melting point $\sim$630°C) with Al impurities migrating into the film during growth. Another possible source of Al is the sapphire substrate (Al_2O_3) where diffusion of Al impurities could occur during elevated temperature growth. This has been reported to occur in the MOCVD growth of ZnO films [80]. Aluminum impurities act as donors in the ZnO film. Thus, it is expected that if there is significant incorporation of Al atoms during growth, charge carrier concentration n, should be relatively high. This is indeed the case as $n \sim 10^{19}$ cm^{-3} was obtained for this sample by Hall effect measurements. The PL results, therefore, confirm the incorporation of Al impurities in our film samples.

For the peak centered at 3.321 eV, it has to be considered that this emission line cannot be assigned to other donor-bound exciton lines as detailed in the Mayer *et al.* review paper. This peak cannot also be assigned as the LO-phonon replica of D^0X peak since the energy separation does not match

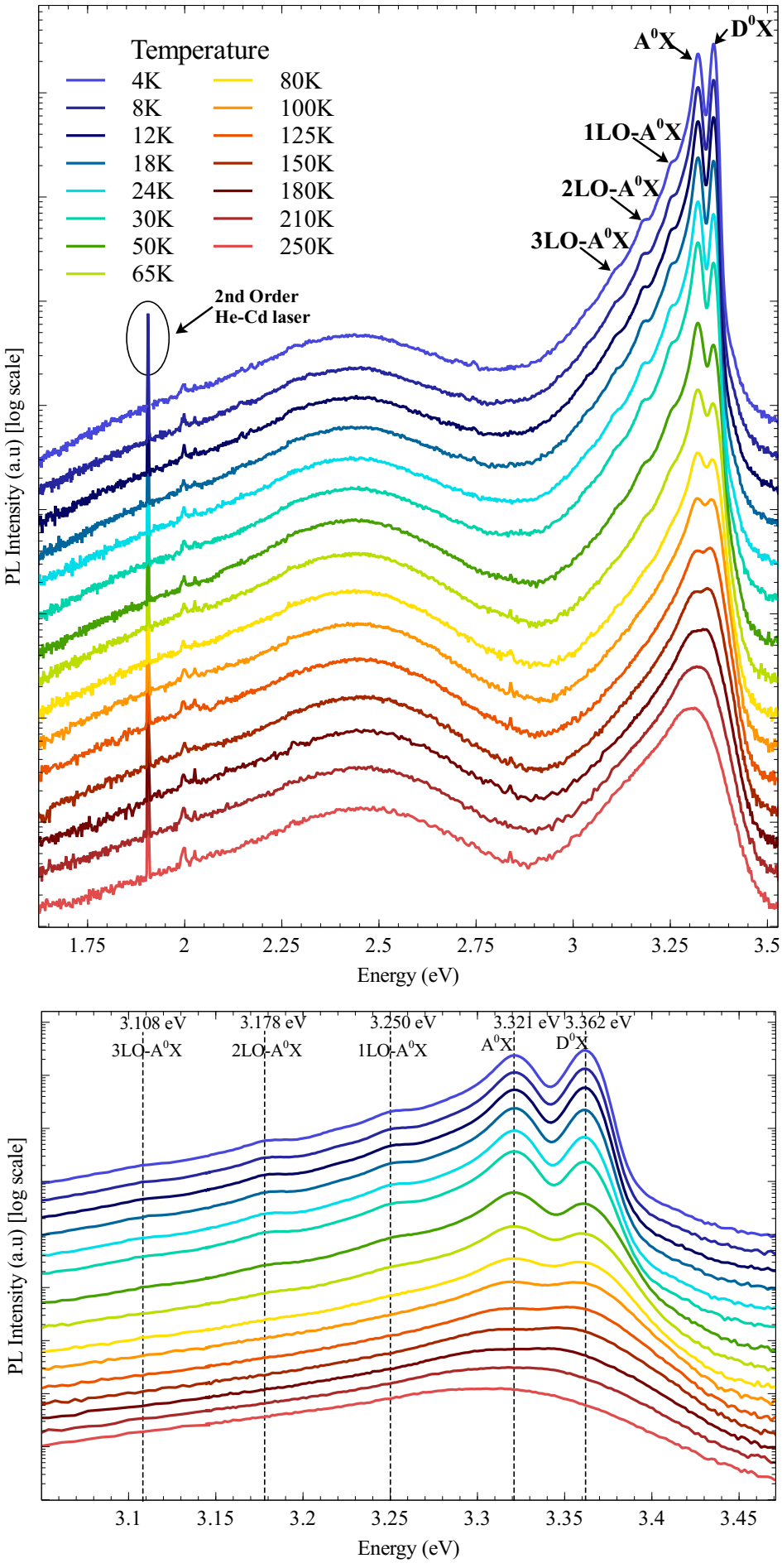


FIGURE 5.10: Temperature dependent PL spectra of as-grown mist-CVD deposited ZnO film on an r-plane sapphire substrate. Vertical offset has been applied to each spectrum for clarity.

the integer multiple of the phonon energy of ZnO. Several papers reported a strong emission line at ≈ 3.32 eV in low-temperature PL spectra of nitrogen-doped ZnO films with N acting as an acceptor impurity. Look and Reynolds [139] observed an A^0X associated emission line at 3.315 eV for homo-epitaxial N-doped ZnO film deposited through MBE. In the PL experiment performed for an undoped and N-doped ZnO samples, Lee *et al.* [129] also observed two prominent peaks at 3.315 eV (assigned to A^0X) and 3.356 (D^0X) for N-doped film, with the absence 3.315 eV emission line for the undoped sample. Further, the work from Ma *et al.* [143] found similar emission lines for N-doped ZnO attributed to D^0X at 3.358 eV and A^0X at 3.317 eV. Similarly, Gao *et al.* [66] assigned A^0X peak at 3.322 eV to nitrogen in N-doped ZnO nanowires. Interestingly, all of these observations assigned the emission peak approximately at 3.321 eV to A^0X originating from substitutional nitrogen in the ZnO crystal lattice. For the spectra shown in Fig. 5.10, the assignment of emission line at 3.321 eV to recombinations from neutral A^0X is the most reasonable as the growth of these ZnO samples used aqueous ammonia as the solvent which provided a nitrogen-rich environment during the growth process.

Also visible on the PL spectra for the sample are peaks attributed to the longitudinal optical (LO)-phonon replicas of the A^0X emission line. The 1st and 2nd peaks are seen on the spectra at 3.250 eV and 3.178 eV while the 3rd is observed at 3.108 eV. These peaks have an energy separation of about 72 meV, corresponding to the phonon energy of ZnO [149]. It is observed that all the phonon peaks on the PL spectra originate from the A^0X emission line with no visible phonon replica of D^0X. This observation is not entirely explainable although it may probably be linked with difference in the binding energies of A^0X and D^0X. However, such observation in PL pattern is very similar to the work of Rommeluere *et al* [189]. In the report, nitrogen incorporated ZnO film grown by metalorganic vapour phase epitaxy showed two A^0X related phonon replicas with no phonon peak associated with D^0X.

The peak corresponding to the free exciton FX is not easily to see in the spectra shown. This may be related to the strong NBE emission lines from D^0X and A^0X originating from to Al and N that dominate the spectra. These NBE peaks are relatively broad (compared with the 2nd order emission from He-Cd laser) which indicates that other point defects may be accompanying them which could induce non-radiative effects that can suppress the free exciton [247]. Temperature-dependent PL shows that emission from D^0X and

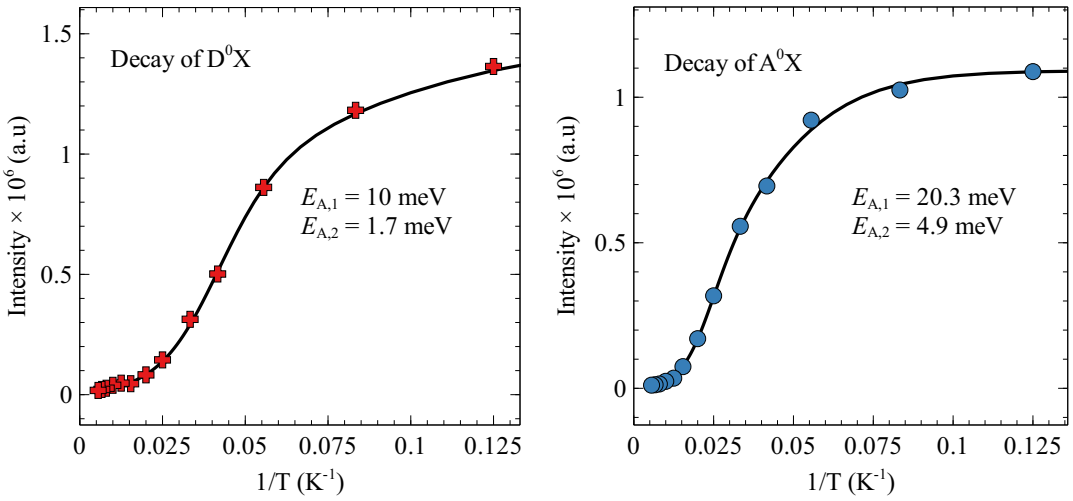


FIGURE 5.11: Arrhenius plots showing the luminescence quenching of D^0X and A^0X as the temperature of the sample increases.

A^0X can be well distinguished at 180 K above which the distinct NBE emission lines merge into an asymmetrically shaped peak as seen room temperature PL spectrum with free excitonic recombination line (FX) expected to dominate the luminescence emission at room temperature. As the temperature increases to room temperature, there is a convergence of the NBE emission lines dominant at low temperatures.

From the above discussion, one may question why p-type conductivity is not evident in these film samples with the incorporation of nitrogen as an acceptor in the lattice, as observed from the PL spectra. An explanation is that nitrogen atom is similar in size to oxygen [176] and can be incorporated either in atomic or molecular states. It is generally considered that the atomic form of nitrogen is preferred for forming p-type doping in ZnO when it substitutes for oxygen. However, with the relatively high energy of the N $\equiv$ N bond ($\approx$ 9 eV), dissociation into atomic form for incorporation becomes unlikely [225, 247]. Instead, the introduction of a nitrogen-rich environment during growth leads to the formation of N_2^- molecule at an O site, thereby leading to compensation as opposed to p-type doping.

The temperature quenching of luminescence intensity can be modelled by the fit to the Arrhenius equation [175]

$$I(T) = \frac{I_0}{1 + A\exp^{-E_{a,1}/kT} + B\exp^{-E_{a,2}/kT} + ...} \tag{5.4}$$

where *I(T)* is the PL luminescence intensity at temperature of T and I_0 is the intensity at low temperature. The terms A and B are dimensionless free fitting parameters and E_a is the activation energy in the thermal quenching process. The number of exponential terms on the denominator correspond to the number of non-radiative decay paths of the transition with activation energies $E_{a,1}$ and $E_{a,2}$. In the simplest form, only a single activation energy is required. However, there is a significant improvement in the fit with a second exponential term in the equation. By fitting with two activation energy terms to the D^0X emission as shown in Fig. 5.11, two activation activation energy values of 10 meV and 1.7 meV are found for the D^0X peak. The higher activation energy is most associated with the localization energy of 15 meV for excitons bound to Al donors [149]. Similar reports on temperature quenching analyses have returned values of 10 meV [149] and 14 meV [75] for emission line of donor bound excitions D^0X. Other non-radiative processes affecting the PL intensity such as hole trapping by low energy native defects is manifested in the second activation energy term.

For the decay of the A^0X emission line, a higher activation energy value of 20.3 meV is derived from the fit to the experimental data. Based on the Haynes rule, the link between activation energy and acceptor binding energy $E_a/E_A \sim 0.1$ for ZnO materials [129], which gives an estimate of acceptor binding energy value E_A = 203 meV for the sample. This value is close to the binding energy of 190 meV which is consistent with shallow acceptor in nitrogen doped ZnO materials [212]. Mathematical model disagreement with theoretical values may be associated with systemic errors in obtaining the PL intensity, including data averaging from overlapping peaks at higher temperatures.

5.5 Summary

Transmission/absorption properties of mist-CVD grown films investigated using transmission spectroscopy show strong photon absorption at photon energy above the bandgap of ZnO. Estimate of bandgap energy ranges between 3.27 - 3.32 eV depending on film thickness.

Temperature dependent transmission shows the bandgap energy depends on the crystal temperature and is blue shifted as the temperature

decreases. Models that quantify bandgap energy shifts with temperature fit well with our experimental data with model parameters comparable with reported values in the literature.

Annealing ZnO film sample in O_2 atmosphere is observed to improve crystalline quality with enhancement of excitonic related peaks post annealing.

An attempt to expand the bandgap of ZnO by doping with Mg did not yield satisfactory results in the mist-CVD technique. Despite a slight increase in bandgap energy after doping, the changes do not follow the bowing relation for $Mg_yZn_{1-y}O$ alloy.

Luminescence properties of ZnO film was studied using PL spectroscopy. Room temperature PL spectrum typically show a strong UV emission peak in addition to a weaker, broad peak in the visible region. PL spectrum acquired at 4 K shows that the UV emission peak comprises two defect related emission lines centred at 3.362 eV and 3.321 eV assigned to D^0X and A^0X respectively.

Chapter 6

MESFET Theory and Fabrication

6.1 Introduction

Transistors are the cornerstone of modern electronic appliances and have become ubiquitous in recent years with the rise in the use of smartphones, televisions, digital displays and various forms of portable electronic devices. A transistor is made from a semiconducting material and is used for amplification or switching of an electrical signal. Multiple connections of transistors in an integrated circuit can perform different logic tasks and function as amplifiers, microprocessors, and computer memory. Transistors are roughly grouped into two categories - Bipolar Junction transistors (BJP) and Field Effect Transistors (FET).

This chapter presents the physical principles in the operation of a metal-semiconductor field-effect transistor (MESFET), a type of a FET structure. Because MESFETs utilize a rectifying metal-semiconductor junction (Schottky) for the gate and a non-rectifying ohmic contact for the source and drain electrodes, the concept of a metal-semiconductor junction is discussed first. Additionally, an explanation of processes undertaken to fabricate MESFET structures on ZnO films grown through the mist-CVD growth technique is presented.

6.2 Metal-Semiconductor Junction

A metal-semiconductor (M-S) contact is important in semiconductor devices - it can act as either a Schottky contact barrier with a rectifying characteristic or an Ohmic contact with non-rectifying current-voltage behavior. The nature of the contact is determined by the combination of the metal and semiconductor materials that form the interface. The description of physical principles that lead to the formation of ohmic and Schottky contacts is presented.

6.2.1 Ohmic contact

An ohmic M-S contact has a negligible resistance relative to the bulk resistance of the semiconductor and ideally has no current rectification properties and no potential barrier for the flow of charge carriers across the interface. Typical M-S that is ohmic has a small voltage drop irrespective of the current level and polarity.

The ability to form an ohmic behavior on an M-S junction is dependent on the work-functions of the metal and semiconductor that form the junction. The work function of a metal $q\Phi_m$ is defined as the minimum energy required to completely remove an electron from the metal into free space also called vacuum level. Work-functions are intrinsic properties of metals and typically range between ∼2 - 6 eV for most metals. Similarly, the work function of a semiconductor $q\Phi_s$ is the energy difference between the vacuum level and the semiconductor Fermi level. The barrier height of the M-S system is determined by the difference in the respective work functions of metal Φ_m and semiconductor Φ_s. A typical ohmic contact can be formed by choosing a metal with $\Phi_m < \Phi_s$ for an n-type semiconductor or $\Phi_m > \Phi_s$ in case of p-type semiconductor material. A low resistance ohmic contact is achieved if the M-S system has a barrier height that is small compared to $k_B T$. In such a combination, current can flow between the metal and semiconductor with little restriction in both directions.

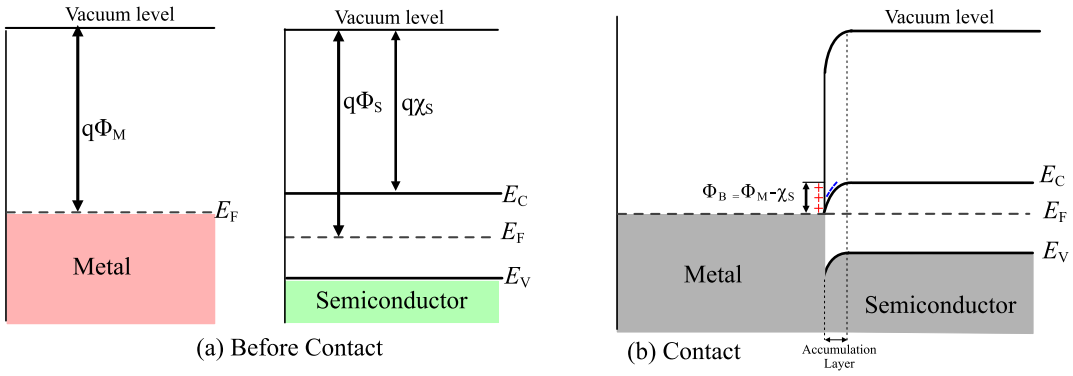


FIGURE 6.1: Energy band diagrams of a metal and n-type semiconductor with $\Phi_m < \Phi_s$ (a) before contact and (b) formation of an ideal ohmic contact.

An energy band diagram leading to the formation of Ohmic contact is illustrated in Fig. 6.1. Before contact is established between a metal and a semiconductor, the different positions of the Fermi levels imply that the

average total energy of electrons in the metal is higher than the semiconductor. To lower their energies, electrons from the metal move to the semiconductor. This electron transfer causes the Fermi level of the semiconductor to move upwards and align with that of the metal to establish equilibrium. This electron transfer from metal to the semiconductor leads to the accumulation of electrons near the semiconductor surface, forming an accumulation layer. In the accumulation layer, the energy band distorts continuously due to the electric field created between the metal and semiconductor arising from charge transfer. This is termed band bending. In an ohmic contact, since $\Phi_m < \Phi_s$, the energy bands bend down towards the interface. As the electron from the semiconductor experiences attraction from a positive charge at the surface of the metal, its potential energy decreases resulting in downward band bending. Due to the absence of a potential barrier for electrons flow from semiconductor to metal, even a small forward bias voltage will lead to a resultant forward current following Ohm's law. A very small barrier is formed for the electron to flow from metal to semiconductor but this small barrier is overcome as the reverse bias voltage increases.

Ohmic contacts can also be achieved alternatively through a tunnel contact by highly doping the semiconductor such that charge carriers can readily tunnel across the barrier separating the metal from the semiconductor interface. Ohmic contact via charge carrier tunnelling is achieved at doping density of $\sim 10^{19}\,\mathrm{cm}^{-3}$ and above [210].

6.2.2 Schottky Barrier

In a Schottky junction, there is ideally a non-linear flow of current through the junction (rectifying contact). In theory, an ideal Schottky junction is formed by a metal of high work-function contacting an n-type semiconductor material. The electrons from the semiconductor reduce their average energy by moving from the semiconductor to the metal leading to a downward movement of the Fermi level. In the absence of surface states, the barrier height Φ_{Bn} of a junction made of metal and n-type semiconductor is given as the difference between the work function of the metal $q\Phi_m$ and the electron affinity of the semiconductor $q\chi_s$.

$$q\Phi_{Bn} = q(\Phi_m - \chi_s) \tag{6.1}$$

The electron affinity of the semiconductor $q\chi_m$ is the difference in energy between the bottom of the conduction band and the vacuum level. The relation

between the work function and the electron affinity of a semiconductor is given by

$$q\Phi_s = q\chi_s + (E_c - E_F) \tag{6.2}$$

with $(E_c - E_F)$ is the energy difference between the Fermi level and the conduction band under the flat band or zero field condition.

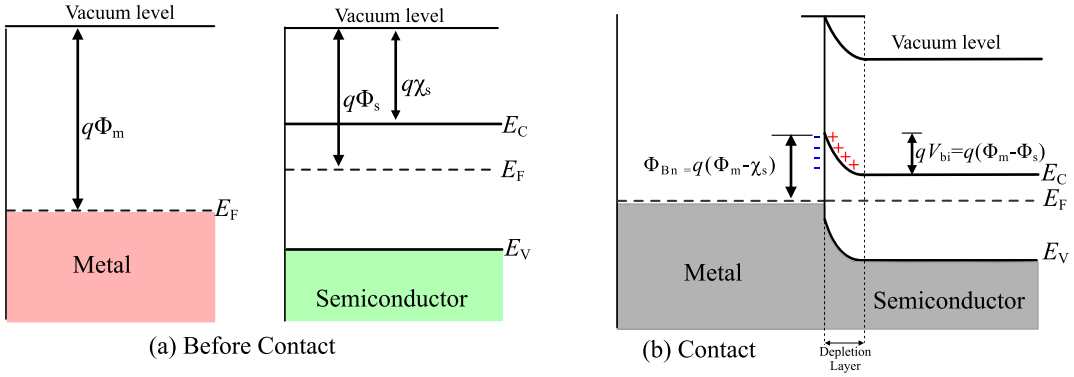


FIGURE 6.2: Energy band diagrams of a metal and n-type semiconductor with $\Phi_m > \Phi_s$ (a) before contact and (b) after formation of an ideal Schottky contact.

The diagram in Fig. 6.2 illustrates energy band diagrams for a metal and n-type semiconductor with $\Phi_m > \Phi_s$, depicting formation of a Schottky barrier. When a metal and a semiconductor are far away and isolated from each other as shown in Fig. 6.2(a), the average energy of the electrons in the semiconductor is greater than that of the metal. When brought into perfect contact (with no surface energy states), electrons from the semiconductor lower their energy by flowing from the conduction band of the semiconductor into the metal. This charge build-up in the M-S interface leads to band structure deformation (band bending) such that the Fermi levels of the semiconductor and metal reach equilibrium and coincide with each other as represented in Fig. 6.2(b). The lowering of the semiconductor Fermi level relative to the metal is equal to the energy difference between their work-functions called built-in-voltage V_{bi} and given by,

$$qV_{bi} = q(\Phi_m - \Phi_s) \tag{6.3}$$

This band bending creates a potential barrier that electrons must overcome to flow from the semiconductor into the metal.

This electron movement from the semiconductor to the metal in contact simultaneously creates an electric field due to the negative charges on the surface of the metal that is balanced by equal but opposite positive charges

on the semiconductor. Thus, a region near the M-S interface is produced in the semiconductor with no conduction electrons - this region is depleted of conduction electrons and is called a depletion layer or space charge region. The formation of a depletion layer in the semiconductor is a vital condition for the achievement of a Schottky rectifying junction The overall effect of the M-S contact is that an electron at the Fermi level of metal faces a potential barrier towards the semiconductor that is equal to the difference between Φ_m and χ_s given by Eq. 6.1. On the other hand, an electron in the semiconductor has to overcome a potential barrier towards the metal that is equal to the built-in-potential V_{bi}.

Forward Bias: The effect of applying voltage bias across the M-S junction is shown in Fig. 6.3. When a forward bias voltage V_a is applied across the junction by connecting the positive terminal of a battery to the metal contact, there will be reduction in the band bending and a resulting decrease in the width of the depletion layer, thus decreasing the barrier for electrons flowing from the semiconductor to the metal from qV_{bi} to $q(V_{bi} - V_a)$. During forward bias, the Fermi energy of the metal becomes lower than that of the semiconductor resulting in the reduction of the potential barrier Φ_{Bn} across the M-S junction. Thus, electrons can easily flow from the semiconductor to the metal due to the reduction in the barrier by the applied forward bias voltage V_a.

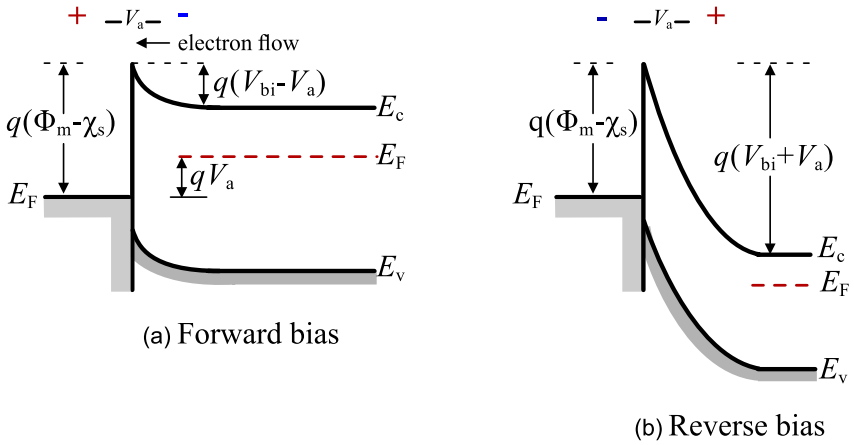


FIGURE 6.3: Effect of applied bias voltage for an ideal M-S contact with $\Phi_m > \Phi_s$ when the contact is (a) forward biased (b) reverse biased.

Reverse Bias: In a case where the metal contact is connected to a negative terminal of a battery and the semiconductor to the positive, there will be an

increase in the band bending and also on the width of the depletion layer. The increased barrier by the applied reverse voltage V_a means that the number of electrons with sufficient energy to cross from the semiconductor to the metal decreases thus, making it more difficult for electrons to flow from the semiconductor to the metal.

6.2.3 Current Transport across a Schottky junction

The dominant current mechanism through a Schottky junction is thermionic emission of electrons across a potential barrier. The thermionic emission theory assumes that the barrier height is much larger than thermal energy $k_B T$ and that thermal equilibrium is established in the system. Also, the model assumes that thermal equilibrium is not distorted by the flow of current across the junction. At room temperature, there is a non-zero probability of electrons with energy sufficient enough to overcome the potential barrier. The current resulting from the flow of electrons from semiconductor to metal is given by the concentration of electrons with kinetic energy sufficient to overcome the potential barrier into the metal.

Under equilibrium and in the absence of an external bias voltage, the current density due to electrons flowing from semiconductor to metal $J_{m\to s}$ is balanced by the reverse current due to electrons flowing from metal to the semiconductor $J_{s\to m}$. Thus under equilibrium condition, $J_{m\to s} = -J_{s\to m}$. Based on the thermionic emission theory, for a Schottky barrier that is much higher than the thermal energy $q\Phi_{Bn} \gg k_B T$, the current density from the metal to the semiconductor under a forward bias applied voltage is expressed as [210],

$$J_{m\to s} = A^* T^2 \exp\left(-\frac{q\Phi_B}{k_B T}\right) \exp\left(\frac{qV_a}{k_B T}\right) \tag{6.4}$$

where V_a is applied forward bias voltage to the Schottky contact and A^* is the effective Richardson constant for thermionic emission given as

$$A^* = \frac{4\pi q m^* k_B^2}{h^3} \tag{6.5}$$

where m^* is the effective mass of the electron. On the other hand, the current density $J_{s\to m}$ due to electron flowing from metal into the semiconductor remains constant, since the barrier height from metal to semiconductor remains unchanged and unaffected by the applied forward bias voltage. Thus $J_{s\to m}$ is equal to $J_{m\to s}$ at equilibrium (i.e. $V_a = 0$). By setting $V_a = 0$ in Eq.

6.4,

$$J_{s\to m} = -A^* T^2 \exp\left(-\frac{q\Phi_{Bn}}{k_B T}\right) \tag{6.6}$$

The total current density J_n is given by the sum of Eqs. 6.4 and 6.6.

$$J_n = J_{m\to s} + J_{s\to m} \tag{6.7}$$

$$= \left[A^* T^2 \exp\left(-\frac{q\Phi_{Bn}}{k_B T}\right) \exp\left(\frac{qV_a}{k_B T}\right)\right]\left[\exp\left(\frac{qV}{k_B T}\right) - 1\right] \tag{6.8}$$

$$= J_0\left[\exp\left(\frac{qV_a}{k_B T}\right) - 1\right] \tag{6.9}$$

where J_0 is the saturation current density given by

$$J_0 = A^* T^2 \exp\left(-\frac{q\Phi_{Bn}}{k_B T}\right) \tag{6.10}$$

Eq. 6.8 shows the dependence of current with applied forward bias voltage in a homogenous Schottky barrier with no surface defects. However, it does not account for some of the deviation from the ideal characteristics due to factors such as image force lowering and effects of interface states [24]. To account for these non-ideal characteristics, an ideality factor term η is introduced to Eq. 6.8 leading to

$$J = J_0\left[\exp\left(\frac{qV_a}{\eta k_B T}\right) - 1\right] \tag{6.11}$$

The ideality factor is a performance metric that accounts for the performance of the Schottky barrier with respect to what is expected in the ideal case with large values indicating deviations and/or inhomogeneous Schottky contacts. Typical values of ideality factors extracted for Schotky diode on bulk ZnO ranges between η = 1.03 - 1.86 [244].

6.2.4 MESFET

A MESFET is a type of FET that employs a rectifying Schottky contact as a gate electrode to modulate device input current. Unlike bipolar transistors, all FETs are unipolar requiring only a particular type of charge carrier (either electrons or holes) for current flow. Additionally, FETs are voltage controlled devices, where the gate voltage switches and modulates output current as opposed to a bipolar junction transistor where the base current controls switching activities. A FET acts like a switch and allows current to

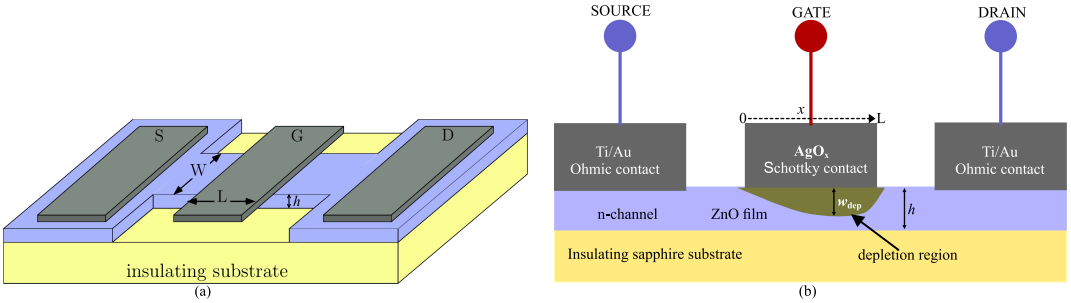


FIGURE 6.4: (a) Schematic diagram showing a MESFET structure fabricated a layer of semiconductor material. Dimensions such as gate length L, gate width W and thickness of semiconductor channel h are shown (b) MESFET with source-drain voltage (V_{SD}) less than saturation source-drain voltage $V_{SD,sat}$ with a depletion region formed. Current flows only through the undepleted region of the channel.

be modulated, and be switched on or off depending on magnitude and polarity of the applied gate voltage. Other common FET structures include metal-insulator-semiconductor FET (MISFET), metal-oxide-semiconductor field effect transistors (MOSFET) and junction field effect transistors (JFET). The operational principles of these types of FETs can be found in standard textbooks.

It is common to notice in textbooks and other reports the reference to the depth/thickness of the depletion layer as a depletion layer width. This terminology probably has its origin from p-n junctions where the direction of current flow is along the width of the depletion region. To avoid mix-up between "depletion layer width" w_{dep} and the width of the gate W, the term "depletion layer thickness" is used throughout the thesis. Also note the difference between the depletion layer thickness w_{dep} and the thickness of the semiconductor channel h, as illustrated in the schematic diagram in Fig. 6.4(a).

Illustrated in Fig. 6.4(a) is a schematic diagram of a MESFET consisting of a semiconducting channel layer deposited on an insulating substrate with source and drain ohmic contacts. In between the source and the drain is a Schottky gate deposited onto the semiconducting channel. A Schottky barrier discussed in section 6.2.2 controls the current to the drain electrode by changing the thickness of the depletion layer depending on the voltage applied to the gate. This, in turn, controls the current that flows from the

source to the drain. The basic design parameters in the operation of a MESFET include the gate length L, gate width W and the semiconductor channel thickness h. The length of Schottky contact along the channel defines the gate length while the gate width is the width of the channel layer. Figure 6.4(b) shows how a silver oxide Schottky gate forms a depletion region in the n-type ZnO semiconductor channel, and thus restricts current flow between the source and the drain contacts. The detailed operational principle of JFET and MESFET is found in several standard texts. Here, we consider the basic working principle of a MESFET with a thin layer of an n-type semiconductor as the channel material.

6.2.5 *I-V* Characteristics of a MESFET

To model the current and voltage characteristics of the channel, we assume the channel approximation introduced by Shockley which asserts that in the absence of a source-drain bias, the depletion layer thickness is the same as that of a p-n junction diode. For the derivation of *I-V* characteristics of a MESFET, the following assumptions are made (**i**) The direction parallel to the substrate surface is given as the x-direction (**ii**) The doping in the channel is uniform and homogenous (**iii**) The length of the gate is larger than the channel thickness (i.e. $L \gg h$ "long channel approximation) (**iv**) The change in electric field in the vertical direction of the channel is much higher than the lateral direction (i.e. "gradual channel approximation") (**v**) The current flow to the gate contact is negligibly small.

Consider when V_G is constant at 0 V as shown in the diagram of Fig. 6.5. With a small applied source-drain voltage $V_{SD} > 0$, the semiconductor channel behaves like a resistor and the current I_{SD} increases linearly with V_{SD} in accordance with Ohm's law. An increase in V_{SD} causes progressive narrowing of the channel due to voltage drop along the channel and a resulting potential difference leading to an expansion of the depletion layer at the drain side of the channel. Since for any given applied voltage V_{SD}, the voltage along the channel increases from zero at the source to V_{SD} at the drain, the Schottky gate becomes progressively reverse-biased towards the drain. This variation of voltage along the channel causes the thickness of the depletion region to be larger on the drain side of the channel thus constricting channel opening and leading to increased channel resistance. As a result, the drain current I_{SD} increases at a slower rate with respect to V_{SD}.

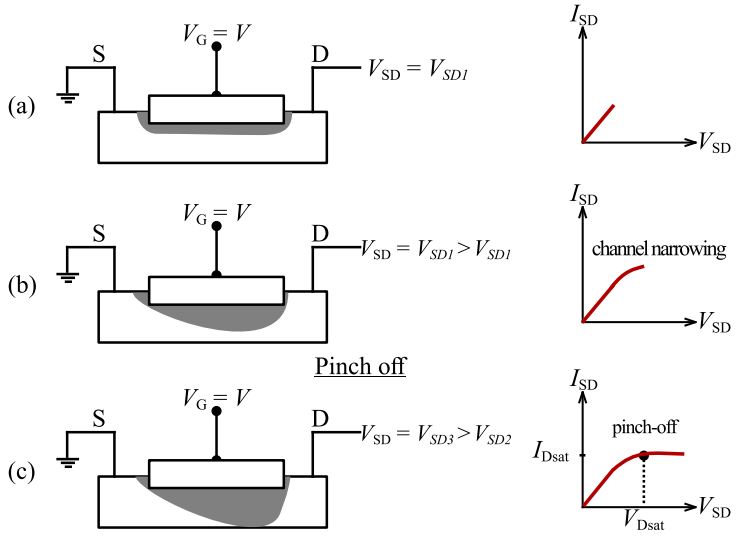


FIGURE 6.5: Effect of increasing V_{SD} at a constant V_G. Further increase leads to pinch-off on the drain side of the channel and saturation of I_{SD}.

If V_{SD} is further increased, the depletion region width continues to expand more especially towards the drain end and eventually completely depletes the channel on the drain side. At the point, the channel is said to be "pinched-off" which leads to the saturation of I_{SD} that it no longer increases with increase in V_{SD}. The V_{SD} at which I_{SD} gets to a saturation level is called the pinch off voltage V_P.

Figure 6.6(a)-(c) is a schematic representation of a depletion mode MESFET with a small and constant V_{SD} applied, that is under increasingly reverse bias gate voltage V_G. In the absence of any gate bias, a uniform depletion region is formed under the gate. If the gate becomes more reverse biased by increasing the negative gate voltage, the depletion region spreads further into the channel and eventually the channel is depleted.

The current flow from the source to drain of the MESFET can be derived by treating the barrier as a resistor that progressively gives a potential drop across the channel. Based on the Shockley theory, the depletion layer thickness w_{dep} in the absence of any bias voltage is similar to that of a one sided p-n junction and written as,

$$w_{dep} = \sqrt{\frac{2\epsilon_s}{qN_D}\left(V_{bi} - V_G\right)} \tag{6.12}$$

where V_{bi} is the built-in voltage and V_G is the forward applied gate voltage across the Schottky barrier. N_D is the donor concentration and ϵ_s is the

dielectric constant of the semiconductor. For the n-MESFET, a positive V_G forward-biases the gate Schottky diode while a negative polarity V_G reverse biases it. The variation of the depletion layer thickness as a function of x

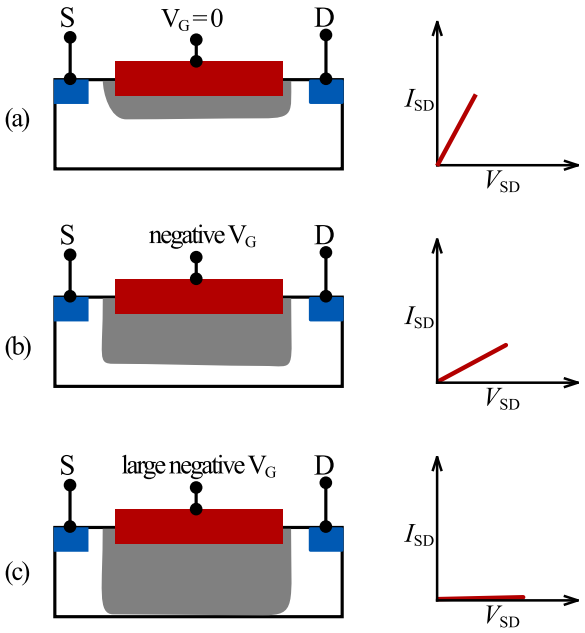


FIGURE 6.6: Schematic representation of a depletion mode MESFET when V_{SD} is small and V_G in increasingly reverse biased.

along the channel is given by

$$w_{dep}(x) = \sqrt{\frac{2\epsilon_s}{qN_D}\left(V_{bi} - V_G + V(x)\right)} \tag{6.13}$$

where $V(x)$ is the potential along the channel. By the schematic representation in Fig. 6.4, the expression for the drain current I_{SD} can be obtained by integrating Ohm's law from the source to the drain.

$$dV = I_{SD}dR \tag{6.14}$$

$$dV = \frac{I_{SD}}{q\mu N_D W(h - w_{dep}(x))}dx \tag{6.15}$$

where $w_{dep}(x)$ is the width of the depletion layer that varies along the channel. By replacing $w_{dep}(x)$ with the expression in Eq. 6.13, we obtain

$$dV = \frac{I_{SD}dx}{q\mu N_D W\left(h - \sqrt{\frac{2\epsilon_s}{qN_D}\left(V_{bi} - V_G + V(x)\right)}\right)} \tag{6.16}$$

The equation above can be rewritten in the form

$$q\mu N_D W \int_0^{V_{SD}} \left(h - \sqrt{\frac{2\epsilon_s}{qN_D}(V(x) + V_{bi} - V_G)} \right) dV = I_{SD} \int_0^L dx \tag{6.17}$$

The solution to the integral gives the expression for I_{SD} when the channel is not pinched off (i.e. I_{SD} not saturated) and is written as [210],

$$I_{SD} = g_0 \left(V_{SD} - \frac{2}{3\sqrt{V_p}} \left[(V_{bi} + V_{SD} - V_G)^{3/2} - (V_{bi} - V_G)^{3/2} \right] \right) \tag{6.18}$$

where g_0 is conductance when the channel is completely open given as

$$g_0 = \frac{q\mu N_D W h}{L} \tag{6.19}$$

and V_p is the pinch-off voltage.

$$V_P = \frac{qN_D h^2}{2\epsilon_s} \tag{6.20}$$

For a MESFET that is normally off (enhancement mode), a positive threshold voltage V_{TH} must be applied to the gate for current to flow and is given by

$$V_{TH} = V_{bi} - V_p \tag{6.21}$$

The above equations are valid in the linear region of the channel that is not pinched-off - i.e. $V_{SD} \leq V_{SD,sat}$. In the case of very low source-drain voltage such that $V_{SD} \ll V_{bi}$ - V_G, Eq. 6.18 can be simplified by using Taylor series to define the drain current in the linear region as [154]

$$I_{SD} = g_0 \left(1 - \sqrt{\frac{V_{bi} + V_G}{V_p}} \right) V_{SD} \tag{6.22}$$

An important performance parameter of the device is the transconductance g_m which defines the change in drain current I_{SD} as a function of gate voltage V_G. It quantifies how well the gate voltage controls the drain current. In the linear regime, the device is ohmic with a transconductance g_m expressed as

$$g_m = \left. \frac{\partial I_{SD}}{\partial V_G} \right|_{V_{SD}} = \frac{g_0 V_{SD}}{2V_p^{1/2}(V_{bi} - V_G)^{1/2}} \tag{6.23}$$

If the V_{SD} is further increased, then the drain current saturates and becomes

dependent only on V_G. This occurs at a state when V_{SD} becomes the saturation drain voltage $V_{SD,sat}$ given as

$$V_{SD,sat} = V_p - V_{bi} + V_G \tag{6.24}$$

By replacing V_{SD} with the drain saturation V_{Dsat}, the expression for the saturation drain current I_{Dsat} is obtained as

$$I_{Dsat} = g_0 \left[\frac{V_p}{3} - V_{bi} + V_G + \frac{2(V_{bi} - V_G)^{3/2}}{3V_p^{1/2}} \right] \tag{6.25}$$

with the transconductance in the saturation region derived from Eq. 6.25 and expressed as

$$g_{m,sat} = g_0 \left[1 - \left(\frac{V_{bi} - V_G}{V_p} \right)^{1/2} \right] \tag{6.26}$$

The model for the MESFET *I-V* characteristics limits the calculation of drain current below the pinch off point of the transistor and assumes a constant current in the saturation region.

The preceding discussion have provided the basic background theory in the operational principles of a MESFET device and some of the vital parameters that influence performance. This background is necessary to understand transistor behaviour when factors such as variation in gate length or width is implemented in a transistor device. Also, experimental measurement in performance metrics of operational transistors can be compared with expected theoretical predictions.

6.3 MESFET Fabrication

The operational principles in a MESFET have been described in the previous section. The discussion in this section will focus on the technique of nano-fabrication required in creating an electronic chip of MESFET devices with various dimensions and geometry. The target electronic chip consists of three-terminal MESFET devices in addition to a few two-terminal Schottky diodes. Also available is a transmission line method (TLM) test structure that is used to determine the contact resistance of ohmic contacts.

The main method employed in the fabrication processes for microelectronic devices presented in this thesis is optical lithography, also called UV lithography or photolithography. This is a micro-fabrication process that transfers geometric patterns using light ($\lambda \approx 0.2 - 0.4\mu$m) from a photomask

to a light-sensitive film on a substrate. This section discusses steps in the fabrication process of MESFETs using mist-CVD grown ZnO as a channel layer.

6.3.1 Description of device layout

One of the very first steps in the fabrication process of a microelectronic device is to create an accurate physical representation of the design in the form of a multi-layer layout. Each layer consists of geometric shapes and dimensions that represent the electronic circuit topology and sizes of components. The geometric shape can represent areas on the semiconducting film to be etched or markers to enhance accurate alignment between different layers of the electronic device. The geometric structures can also represent regions where ohmic or Schottky contacts are deposited on a substrate.

The layout design for microelectronic devices can be accomplished by some graphics editors with some dedicated computer-aided design (CAD) software programs (e.g. Layout Editor, L-Edit, KLayout) best suited for such designs. These dedicated CAD computer programs enable the designer to work on multiple layers that will be represented on the different masks, in addition to hierarchical design features. The hierarchical design feature allows for use of low-level graphical structures as part of higher-level structures.

It is important to decide on the layers for the targeted electronic device, suitable fabrication steps and the number of photomasks that will be required. The design of the microelectronic device reported in this work was done by a former post-doctoral fellow within our research group. The device chip is fabricated using four distinct fabrication steps represented by each layer in the design. A description of each layer of the design layout is presented.

Layer 0 - Alignment markers

This represents the first layer of the design layout. These markers are not vital in the operation of the devices, and fabrication can be done without the markers. However, since ZnO films and sapphire substrates are both optically transparent, the markers ease the task of alignment between different layers. The geometric CAD pattern of the markers is shown in Fig. 6.7. Some considerations need to be made when choosing alignment markers. At least one marker is required on each side of the design layout and must fit within

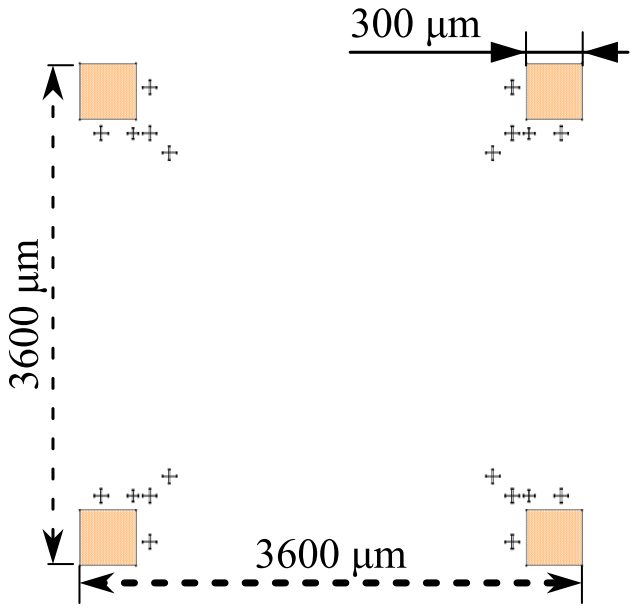


FIGURE 6.7: These markers are used to enhance accurate alignment by matching the positions of markers on each layer.

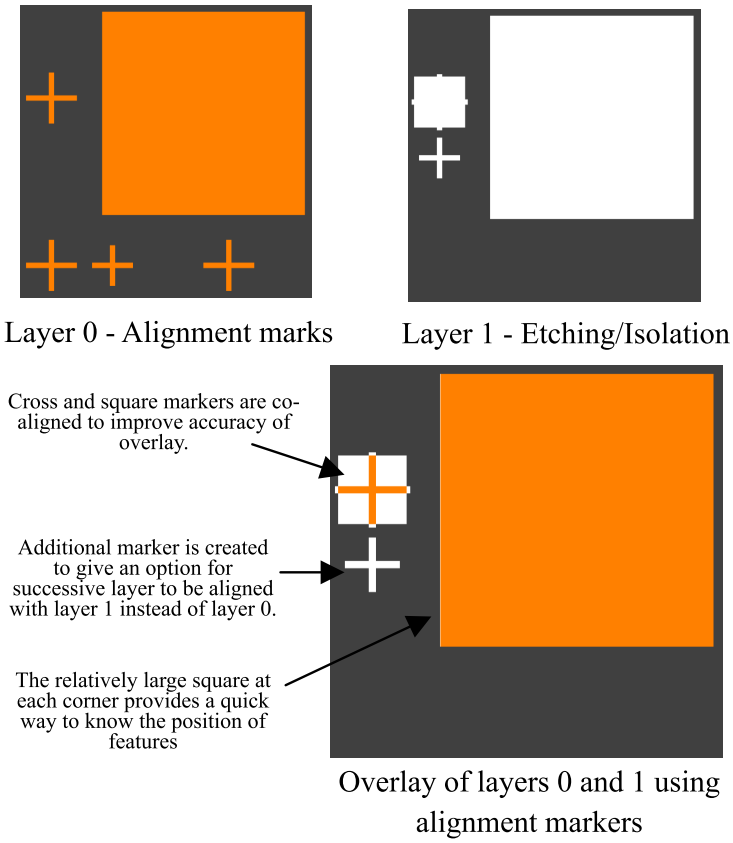


FIGURE 6.8: Illustration of how alignment markers are co-aligned on a layout corner to ensure that layers are accurately overlaid.

the field of view of an aligner's microscope. The marks must also permit accurate alignment in the translational (x,y) and rotational directions.

An illustration of how alignment markers place at a corner of the design is used to ensure accurate overlay of different layers is shown in Fig. 6.8. Alignment features with geometric shapes of a cross and square (with upward kink) are used to accurately align the layers based on visual assessment under the view of a microscope. The large square at each corner is used as a rough alignment feature while the crosses improve alignment accuracy under higher magnification. Each layer of design layout has alignment features placed at each corner to enable alignment with markers on layer 0.

Layer 1 - Etching/Isolation

The MESFET devices need to be fabricated on an active semiconducting channel that is isolated to avoid a cross-talk between conduction paths of adjacent devices. This represents the second layer in which the geometric patterns represent the regions on the semiconducting layer that will be etched off to create isolated conducting paths. Fig. 6.9 represent the geometric pattern delineating regions on the active semiconductor film that is etched.

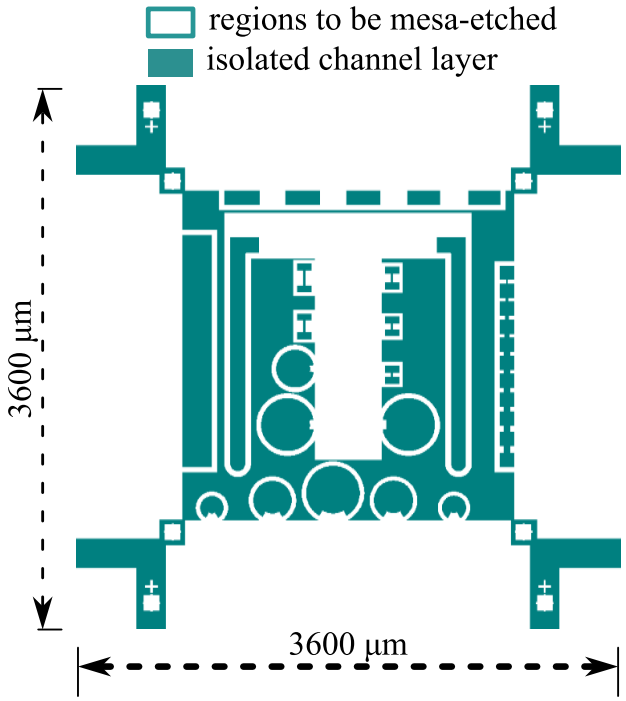


FIGURE 6.9: Pattern that represents film layer mesa-etched to create isolated conducting paths for transistor devices.

Layer 3 (ohmic) and Layer 4 (Schottky) contact metals

The last two layers are patterns for the ohmic and Schottky contact electrodes shown in Figs. 6.10 and 6.11. For MESFETs, the ohmic contact metals are used for the source and the drain while the Schottky contact is the gate. There is no strict order on whether the ohmic or Schottky layer is fabricated first. However, in for this work, the Schottky contact layer is fabricated last to reduce the likelihood of any damage to the Schottky gate, which is critical to MESFETs operation.

So far, the description has been given for the geometric designs that should represent different layers in the final electronics design chip. These geometrical shapes are simply graphics that correspond to the physical dimensions of the transistors and other test structures on the chip. In a so-called "maskless photolithography" technique, these geometric features can be directly written to a wafer/substrate. A paper by Menon *et al.* [147] provides a good review of maskless lithography and emerging applications in research and industries. Currently, the technology for high throughput and high volume maskless lithography in the optical regime is still in its embryonic stages. However, the technology of maskless direct laser writing is already used but for the production of photomasks and limited wafer-level patterning. The traditional method of micro-fabrication using photomasks to transfer patterns to the substrate/wafer was used in this work.

In the mask-based photolithography technique used in the fabrication process for microelectronic devices reported in this thesis, each layer of the design pattern is first written to a photomask which serves as master image/template. The photo-mask is then used to transfer geometric features of each layer onto a wafer using projection lithography. The photomask holds the template of each layer and can be used for multiple fabrications of the same devices with the same design. The next section describes how each layer of the geometric pattern described above is transferred to a photomask that serves as a template for multiple fabrications of devices.

6.3.2 Photomask Fabrication

The core aspects of photomask fabrication involve the use of a laser beam pattern generator that directly transfers patterns to wafer/substrate. A schematic illustration of a laser mask writer is shown in Fig. 6.12. In this work, the Heidelberg μPG 101, a laser-based micro pattern writer for low volume mask making was used to transfer each layer of CAD pattern to a photomask. It

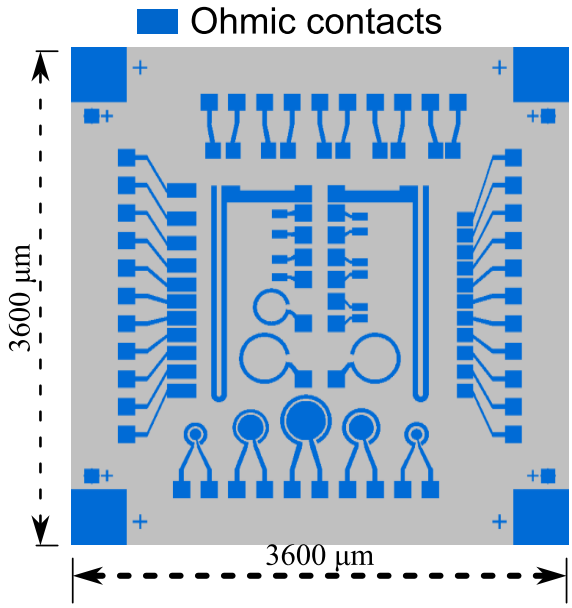


FIGURE 6.10: This layer represents the pattern for ohmic contacts employed as the source and drain electrodes.

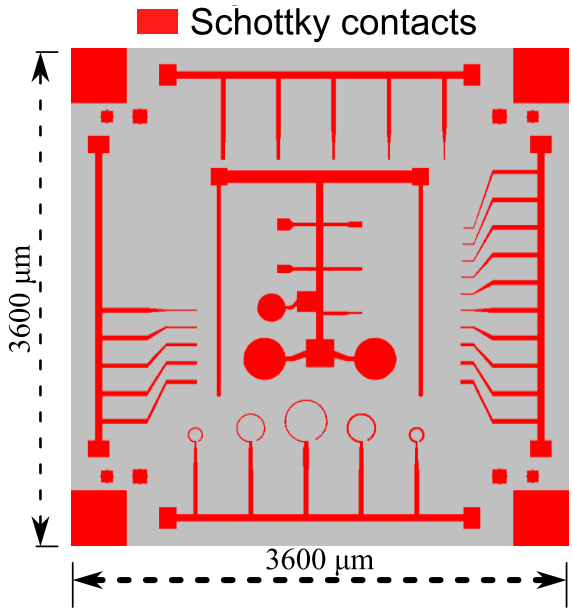


FIGURE 6.11: The Schottky contact layers represent patterns for the gate electrodes.

uses a direct exposure with a laser diode of wavelength 405 nm to transfer patterns on a substrate coated with photosensitive material called a photoresist. This technique is used to pattern each layer of chip design on a photoresist coated blank photomask. Figure 6.13 illustrates the steps in making a photomask to be used for MESFET fabrication on deposited ZnO film.

A commercially available Nanofilm AZ 1518 soda lime low reflective mask blank consists of an opaque coating on top of a substrate that is transparent

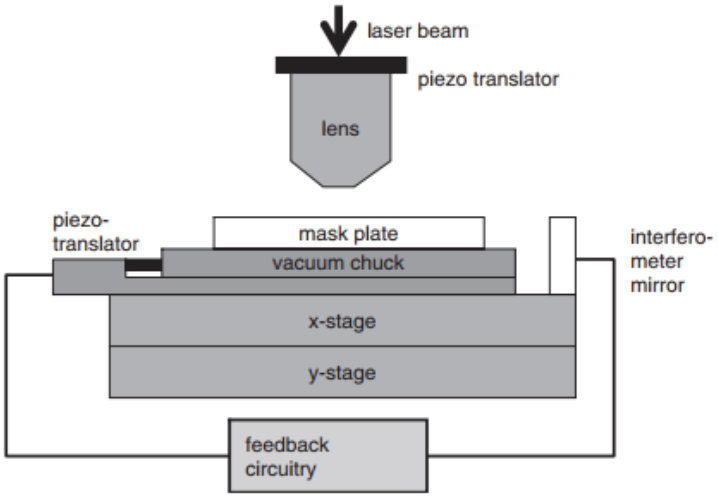


FIGURE 6.12: A mask writer used for transferring geometric designs patterns on a photoresist-coated photomask [56].

to UV light. Typically, quartz glass or soda-lime is used as a substrate due to high transparency in deep UV wavelength and low thermal expansion coefficient. The opaque coating should ideally be a high optical density material, chemically stable and amenable to patterning. The most widely used material for opaque photomask coating is chromium Cr and its compounds. A pure Cr metal layer has high reflectance on both interfaces, with stray light reflections creating potential problems on pattern transfer. Instead, an anti-reflecting coating of chromium oxide is deposited on top of the chromium film. On top of the anti-reflective chromium oxide layer is a thin film of photosensitive material called a photoresist.

Each layer of the geometric design is printed on the blank photomask by a mask writer. After exposure, the geometric designs are created as latent patterns in the photoresist coating. The next process is for the latent design pattern to be developed. This is done by immersing the photomask in a developer chemical (AZ 326 MIF developer) where regions illuminated by a laser get dissolved thereby exposing the chrome layer. Regions on the photoresist layer without laser light illumination remain intact and protect the chrome layer underneath. The next step is the etching of the exposed chromium. A wet etching method was employed by using a chrome chemical etchant, comprising of a mixture of perchloric acid ($HClO_4$) and ceric ammonium nitrate $(NH_4)_2Ce(NO_3)_6$. After etching, the remaining photoresist layer is stripped from the mask plate by ultrasonic agitation in acetone.

With each layer of the desired design of the microelectronic chip held as a template on different photomasks, multiple fabrications of the same chip can

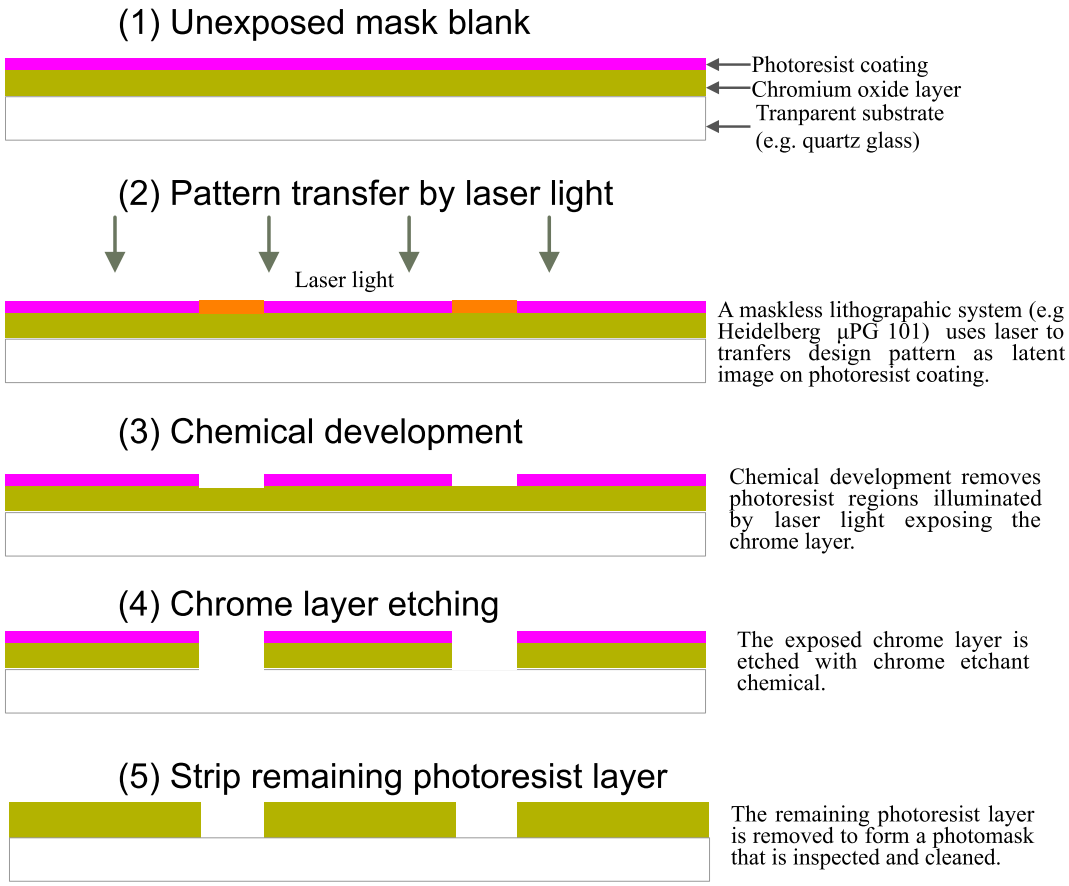


FIGURE 6.13: Schematic illustrating the transfer of geometric pattern on a photomask with a positive photoresist coating.

be performed on mist-CVD deposited ZnO films as semiconductor channel for devices. This process involves additional photolithographic steps using another equipment called a mask aligner, shown in Fig. 6.15 to transfer the design held on the photomask to the ZnO film substrate.

6.3.3 ZnO Substrate Preparation

One of the initial tasks in the fabrication process is the preparation of ZnO film substrate. First, ZnO film is deposited on a 10 mm $\times$ 10 mm r-plane sapphire substrate at a growth temperature of 500°C using the mist-CVD technique. As explained in section 4.6.3, ZnO films deposited on r-plane sapphire substrates generally have smoother surface morphology compared with films grown on c-plane sapphire substrates. A smooth semiconductor layer is desirable for good device functioning by minimizing weak gating effects caused by poor electrical contact between a rough film and a metal. The deposited film is diced into four pieces of 5 mm $\times$ 5 mm film samples. One

of the diced film samples is employed as an active semiconducting channel for the fabrication of MESFET structures and undergoes further microfabrication steps to make electronic devices.

Characterization techniques to study optical transmission, surface topography and electrical properties of the film sample are performed for the deposited film. Once the film properties are known, annealing of the film sample is done at 700°C under an oxygen atmosphere for 30 minutes. Film properties are again studied after the annealing process.

Cleaning the ZnO substrate is vital in the fabrication process. This is because dust particles or other contaminants on the ZnO film or photomask can cause defects in the fabricated device and result in circuit failure. Thorough cleaning is performed on grown ZnO film by ultrasonic agitation for 10 minutes duration each in acetone, methanol, and IPA. Next, a ZnO film is blow-dried using a nitrogen gas gun and securely stored in a thin film box ready for further fabrication steps.

Substrate mounting

Deposited ZnO film, 5 mm $\times$ 5 mm on r-plane sapphire is further mounted on a silicon wafer that is approximately 20 cm $\times$ 20 cm. Mounting the sample on a larger silicon wafer allows for a large surface area necessary for suitable vacuum pressure to keep the sample firmly fixed on the stage of a mask aligner. Additionally, mounting the sample on a silicon wafer improves the

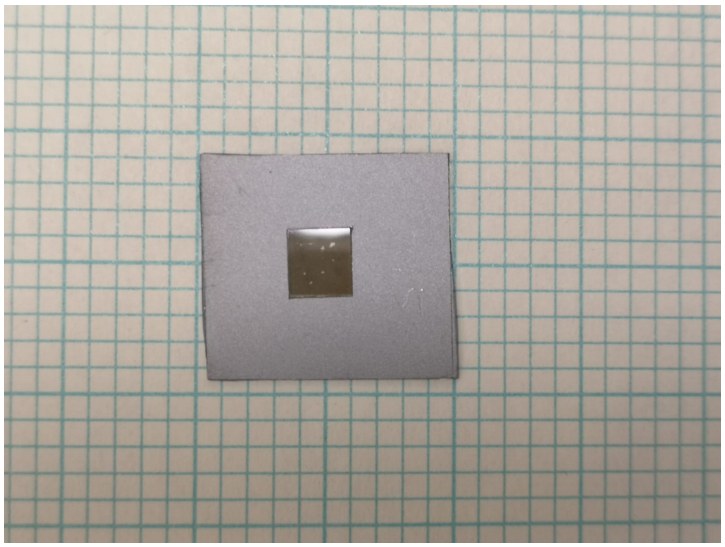


FIGURE 6.14: ZnO film deposited on a sapphire substrate is mounted on a silicon wafer approximately 20 cm $\times$ 20 cm using a tiny drop of photoresist

ease of handling and reduces the risks of damage to the film sample. Fig.

6.14 shows a ZnO film sample mounted on a silicon wafer ready for further fabrication steps. The ZnO film attached to the silicon wafer using a drop of photoresist is then placed on a hot plate set at 96°C for 15 minutes to enable good adhesion between the film sample and the silicon wafer.

Photoresist spin coating

Spin coating is used to evenly spread a layer of photoresist chemical on the ZnO film layer. In this work, a positive photoresist (MicroChemicals AZ1518) for all the optical lithographic procedures reported in this thesis. A spinner accelerated to 5000 rev/min deposits approximately 1.5 μm thickness of photoresist on the ZnO film surface.

The spin-coated photoresist remains wet and therefore requires a soft bake step to remove most of the solvent. In this work, the method of choice for soft bake is to place the photoresist coated ZnO substrate on a hotplate maintained at a temperature of 96°C for 3 minutes and allowed to cool under cleanroom ambient conditions.

6.3.4 Photolithography with the mask aligner

Following spin-coating with a positive photoresist, the mounted ZnO film substrate and a photomask for each layer of fabrication are inserted in a mask aligner. Despite its name, the mask aligner is both used for alignment and exposure with UV light. The mask aligner in Fig. 6.15 is a Karl Süss MA6 mask aligner. It is equipped with lamp, mirror, shutter and lens systems that allow for controlled alignment of substrate and photomask, in addition to a uniform exposure of UV light over the substrate. The mask aligner speeds up fabrication by exposing the photoresist coating of a wafer with UV light, a process that can be completed within seconds in contrast to mask writer which can take up to hours depending on the complexity of the pattern. To transfer the pattern held on a photomask to the ZnO film substrate, the photomask is placed above the ZnO film substrate while UV light illuminates the photoresist-coated ZnO film through the openings of the photomask. This process transfers the pattern held on the photomask to the photoresist coating on the ZnO film. Further chemical treatment is done to expose regions on the photoresist coating illuminated by the UV light thereby exposing some regions on the ZnO film layer for subsequent processes such as metallization or etching. In line with the layout of the electronic design, there are four different photomasks each holding templates of layers in the fabrication process

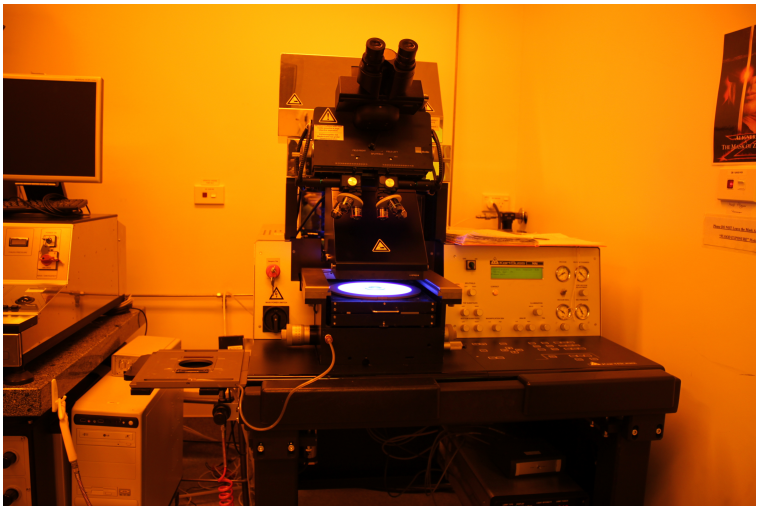


FIGURE 6.15: A Karl Süss MA6 mask aligner used to accurately align a substrate with a photomask. UV light projects through the mask and selectively illuminates the sample coated with a photoresist.

for the alignment markers, etching/isolation layer, ohmic contact electrode, and Schottky gate electrodes.

The illustrations in Fig. 6.16 describe the fabrication steps undertaken from etching the ZnO film layer to the final step of depositing the Schottky gate contact electrodes. Details of each of the fabrication steps will now be presented.

6.3.5 Alignment

Following spin coating by a photoresist layer, the ZnO film substrate and the photomask are inserted into a mask aligner. Alignment is not needed for the first mask layer (i.e alignment markers). However, it is important to print the alignment marks on the substrate to enable subsequent photomasks to be aligned with already existing patterns. The alignment marks are particularly necessary especially when the first fabrication step does not lead to visible features on the ZnO film. For example, etching only removes some regions of transparent ZnO film without any other visible features after the etching process.

The alignment marks comprises a bi-layer of Ti/Au deposited through electron beam evaporation under vacuum. The alignment marks need to be robust and adhere well to the ZnO film substrate to withstand further chemical processes encountered in the fabrication process. The choice of a bilayer of Ti/Au as markers stems from the superior property of Ti in terms

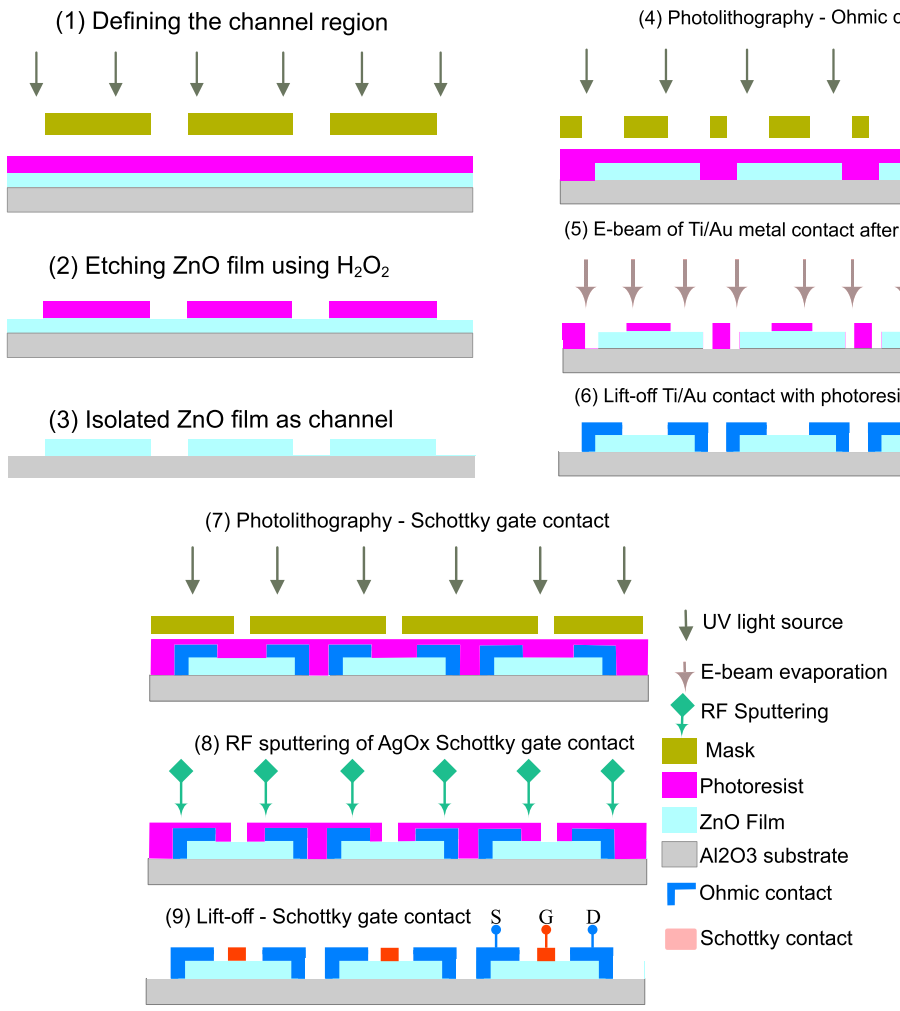


FIGURE 6.16: Schematic representation of fabrication steps involved in making MESFET devices using a thin layer of ZnO film as an active channel.

of its high affinity for oxygen. Unlike most noble metals especially Au, Ti adheres well to oxide films and glass due to its ability to react and form a stable metal oxide at the interface. The Au capping layer prevents oxidation of Ti since oxidized Ti will lead to poor adhesion in the subsequent deposition of Au. Also, Au creates shiny features on a transparent ZnO film background which helps to ease the alignment of successive layers on top of previous layers.

6.3.6 Etching/Isolation

Following photolithography and deposition of alignment markers on the ZnO film substrate (not shown in Fig. 6.16), an etching process is done on the ZnO film layer to create an isolated conducting path as active channels

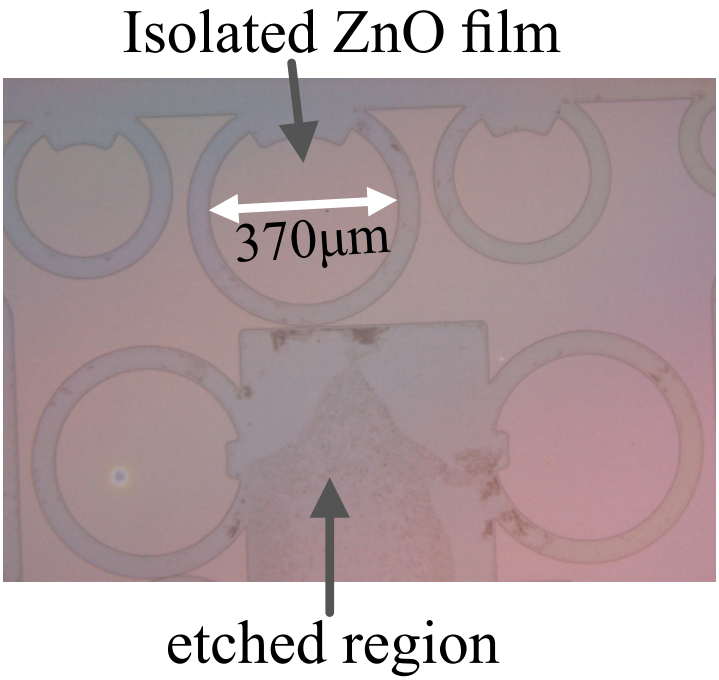


FIGURE 6.17: Optical micrograph of an isolated active conducting channel for a transistor after etching with H_2O_2 solution on a 43 nm thick ZnO film.

for transistor structures. A mesa isolation method was used which requires etching away the conducting film into the insulating substrate thereby preventing lateral conduction between transistor devices.

Based on a recent article [235], a controllable etching of ZnO films was achieved using a solution of hydrogen peroxide H_2O_2. The fabrication step that requires etching of ZnO film followed through with this report by employing H_2O_2 (40 wt.%) for etching ZnO film layer and utilizing it for microelectronic device fabrication. To our knowledge, there are no available research works that have utilized H_2O_2 solution for etching the ZnO conducting layer for making devices. Figure 6.17 illustrates the excellent etching result obtained by wet etching ZnO film sample with H_2O_2. Following photolithography with the photomask which selectively delineates areas of the film to be etched off, the mounted ZnO film substrate is then dipped into a solution of H_2O_2 to remove regions on the film surface exposed from the photolithography procedure. Etching duration was 10 minutes for all devices reported in this thesis. To confirm if the etching process successfully removed the ZnO film from the insulating substrate, a micrometer controlled electrical probe and a parameter analyzer were used to create voltage bias on the etched away region to confirm that no detectable current was measured

on the etched area of the film sample.

6.3.7 Metallization - Ohmic and Schottky Contacts

After creating isolated conducting paths for the transistor structures by the etching process, the next step in the fabrication process is to deposit ohmic contact metal for the source and drain electrodes, as well as Schottky contacts for the gate. Several research works have shown that the effective Schottky barrier height increases for partially oxidized metals, instead of pure metal in ZnO thin films and bulk materials [88, 4]. The deposition of metal contacts was achieved either by electron beam evaporation (for Ohmic contacts) or reactive RF sputtering (for oxidized metal Schottky contact). The conductivity of the Schottky electrode is expected to be substantially lower than that of its pure metals due to oxidation which can cause electrical conductivity to be non-homogeneous across the contact area. By capping the oxidized material with pure metal (e.g Au), a homogeneous and equipotential surface across the contacts is established. Typical deposition conditions for the Ti/Au Ohmic and AgO_x Schottky contacts are shown in table 6.1. Other ox-

TABLE 6.1: Deposition conditions for the Ohmic and Schottky contact electrodes

Source	Material	Gas (sscm)	Power	Base Pressure	Process Pressure	Thickness
E-beam	Ti	-	70 mA	8.4e-6 mbar	3.3e-6 mbar	$\sim$ 50 nm
	Au		36 mA	3.8e-6 mbar	4.0e-5 mbar	$\sim$ 50 nm
RF	AgO_x	Ar (10) O_2 (10)	50 W	8.4e-6 mbar	3.3e-6 mbar	$\sim$ 50 nm

idized Schottky metals deposited under similar conditions as shown in the table include PtO_x, PdO_x and IrO_x. The film deposition system used for RF sputtering and electron beam evaporation of metal and oxidized metal contacts is shown in Fig. 6.18.

For some semiconductor materials that are not attacked by metal etchant chemicals, etching of deposited metal can be employed in the fabrication process. However, ZnO being amphoteric reacts with most metal etchants chemicals. Most metal etchants are acidic and will readily attack and etch the underlying ZnO material. A more suitable patterning method involving lift-off was therefore used.

In a lift-off etching process, a photoresist layer is spin-coated on the ZnO substrate followed by standard photolithography to lay open the area where the metal contacts will be deposited. Metal layers are then deposited on the

ZnO film substrate either by electron beam evaporation (Ti - Ohmic contact) or sputtering (e.g. AgO_x - Schottky contact). After deposition, the sample is immersed in acetone which dissolves the photoresist leaving behind the deposited metal contacts that adhered directly to the ZnO film. Metal deposited on the photoresist protection layer flakes/lifts off when the photoresist layer is dissolved and stripped by acetone.

In a lift-off process, care is taken to prevent bridging that occurs when a deposited metal layer that adheres to the surface of the conducting film and photoresist. Bridging effect prevents a good lift-off process and can make fabricated devices non-functional due to cross-talk between adjacent contacts. By using a photoresist layer with a thickness that is substantially higher than the deposited layer enables a reliable lift-off process to be achieved. Our spin-coated photoresist layer is $\sim$1.5 μm while the bi-layer of deposited metal contact is $\sim$100 nm. Even in a situation of minor bridging, methods like ultrasonic agitation of the sample in acetone can remove bridging and give a good lift-off profile.

Ohmic Contact Metal

The source and the drain electrodes of a MESFET are ohmic contacts that take current in and out of the semiconducting material and should ideally have high heat dissipation and low contact resistance to improve device performance and efficiency. All fabrication processes presented in this thesis used a bi-layer of Ti and Au successively deposited in vacuum through electron beam evaporation. This combination of the Ti/Au layer has often been used for the ohmic contact electrodes in oxide thin-film transistors [14, 238, 234] and was noted to provide low specific contact resistance to ZnO-based semiconductor channel layers [91]. Also, Ti is reactive towards ZnO with a high affinity for oxygen atoms compared to zinc. Therefore, Ti forms an interfacial layer when it reacts with oxygen in ZnO material. This results in the movement of oxygen atoms from the ZnO material into the Ti metal, thereby creating oxygen vacancies. Oxygen vacancies are well reported to contribute to n-type conductivity in ZnO; therefore, more n-type charge carriers become available leading to a further reduction in barrier height for the ohmic contacts.

The Au metal deposited on top of the Ti serves as a capping layer to prevent oxidation of Ti and protect the ohmic contact from potential damages when measuring devices with pointed probes.

FIGURE 6.18: A sputtering machine used for RF sputtering of Schottky contact and deposition of metallic contact by electron beam evaporation.

Schottky Contact Material

According to the theory of M-S junctions described in section 6.2, a rectifying Schottky contact is formed between a semiconductor and a metal with work function Φ_m higher than the semiconductor Φ_s. Rectifying M-S junction made with noble metals such as Au, Ag, Pt and Pd have been achieved in some semiconductor materials. In the case of ZnO, attempts to make reliable rectifying Schottky contact with metals have resulted in defective rectifying contacts characterized by high reverse leakage current, high ideality factor, and low barrier heights [218].

It has been demonstrated that a good quality Schottky contact is achieved with non-stoichiometric silver oxide on a single crystalline ZnO substrate rather than metallic silver [2]. Similarly, improved performance of Schottky contact with oxidized silver metal on hetero-epitaxial ZnO film grown on a sapphire substrate has been reported [126]. Many of the few works available in the literature that compared performance parameters of different Schottky contacts made from noble metals have shown that Ag has a higher barrier height compared to other metals [57, 51]. It was, therefore, natural to consider silver oxide as the first choice of Schottky contact material for MESFET

fabrication.

Reactive RF sputtering with oxygen gas was used to deposit the Schottky contact to form metal oxides. According to Allen *et al,* [4], oxidation of the Schottky metal leads to a significantly lower conductivity compared with its pure metal form. Therefore, a metallic capping layer usually electron beam evaporated gold provides a low resistance contact to the actual Schottky electrode and forms an equipotential surface. The capping layer also serves to protect the Schottky electrode from scratches when measurements are done with the needle-like probes.

The oxygen used in the sputtering process is reported to offer some benefit in Schottky contact performance. Firstly, the bombardment of negatively charged oxygen ions at the initial stage of the sputtering process leads to surface pre-treatment of the channel semiconductor before the actual deposition of the contact electrodes. Additionally, it is suggested that oxygen ions remove monolayers of hydroxide species which form accumulation layers that increase surface conductivity and impact on the device performance such as leakage current and barrier height [33].

6.3.8 Completed Chip

Micro-fabrication is completed with the fabrications steps involving photolithography accompanying depositions of ohmic and Schottky contact electrodes. The alignment of each layer of the device is very important and care is taken to ensure accurate overlay of each layer using the alignment markers. Even a slight misalignment can potentially render some of the devices non-operational. It is also desirable to have transistors with a range of different sizes and dimensions since the actual characteristics of devices being fabricated are somewhat unknown. Transistors with different dimensions and shapes increase the likelihood of fabricating one with ideal or even measurable performance, and enable one to study the effects of varying geometry and dimension on performance. The vital parameters in the dimension of a transistor are the width and length of the gate.

The fabricated microelectronic device chip, with the micrograph shown in the upper central area of Fig. 6.19 measures 3600 μm $\times$ 3600 μm and consists of transistors and Schottky diodes with varying gate length, gate width, and geometries. These variations on transistor test structures enable the effect of design parameters to be studied and investigated.

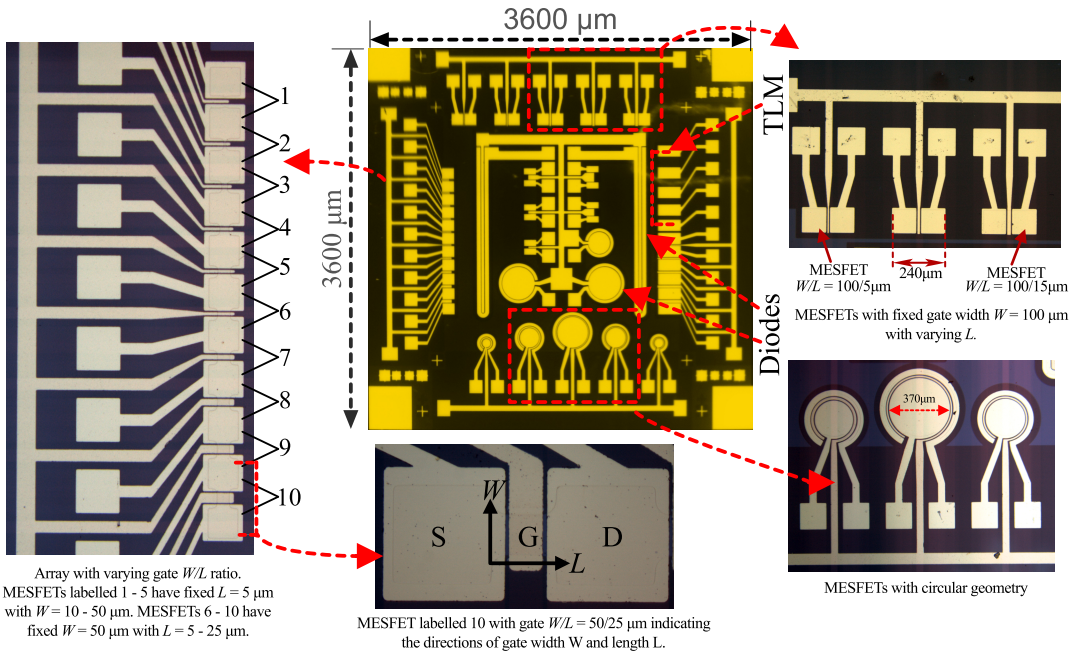


FIGURE 6.19: Micrograph of fabricated microelectronic device chip with area 3600 $\times$ 3600 μm^2 showing MESFETs with the varying gate lengths, widths, and geometries including diodes and TLM structure.

Also available on the fabricated electronic chip is an array of ten MESFET structures labelled from 1 to 10 with variations in dimensions of gate width and length as shown on the left side of Fig. 6.19. The first five structures (labelled 1 - 5) are transistors that share a fixed gate length of 5μm, with a progressive increase in the gate width from 10 μm - 50 μm. The five other transistor structures, labelled 6 - 10 in the array have a common gate width of 50 μm and a progressive increase of gate length from 5μm - 25 μm. This array is used to examine the effect of gate *W/L* ratio on the performance characteristics of MESFETs.

Another array on the chip shown on the top right of Fig. 6.19 consists of five MESFET devices (micrograph of three are shown). The gate width for the MESFET devices is 100 μm while the gate length varies from 5 μm - 25 μm. This array was selected to determine the effects of varying gate length at a fixed gate width on the performance metrics of MESFETs. In reference to the schematic diagram of a MESFET structure in Fig. 6.4(a), it is important to note that gate length is defined by the length of the metal contact along the etched semiconductor channel from the source to the drain. Conversely, the width of etched semiconductor layer without considering any overlapping contact metal across the channel represents the gate width. The zoomed micrograph of MESFET number 10 in Fig. 6.19 illustrates that visualizing

the gate width may not be obvious since the etched semiconductor layer is directly overlaid by the gate metal, that overlaps along its width.

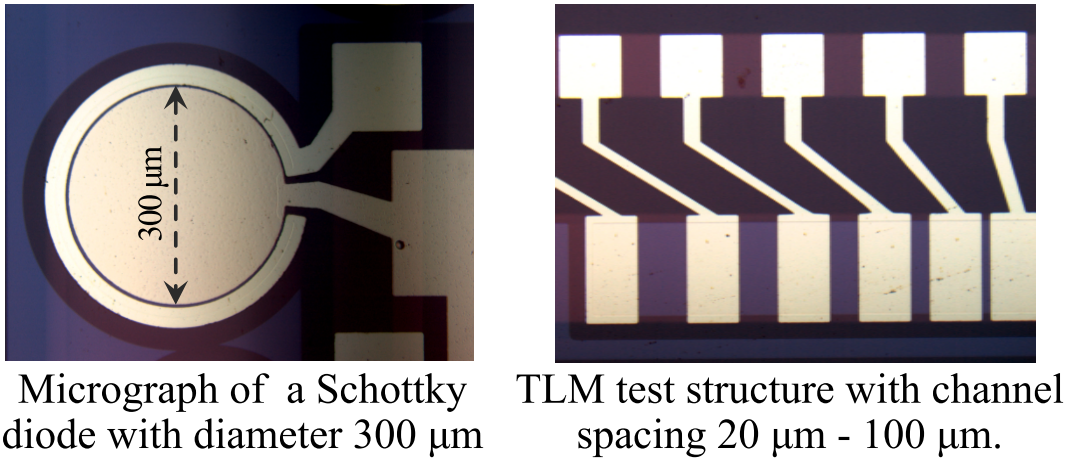


FIGURE 6.20: Zoomed micrographs of a Schottky diode for *C-V* measurement and a transmission line method (TLM) structure for determining contact resistance of ohmic contacts.

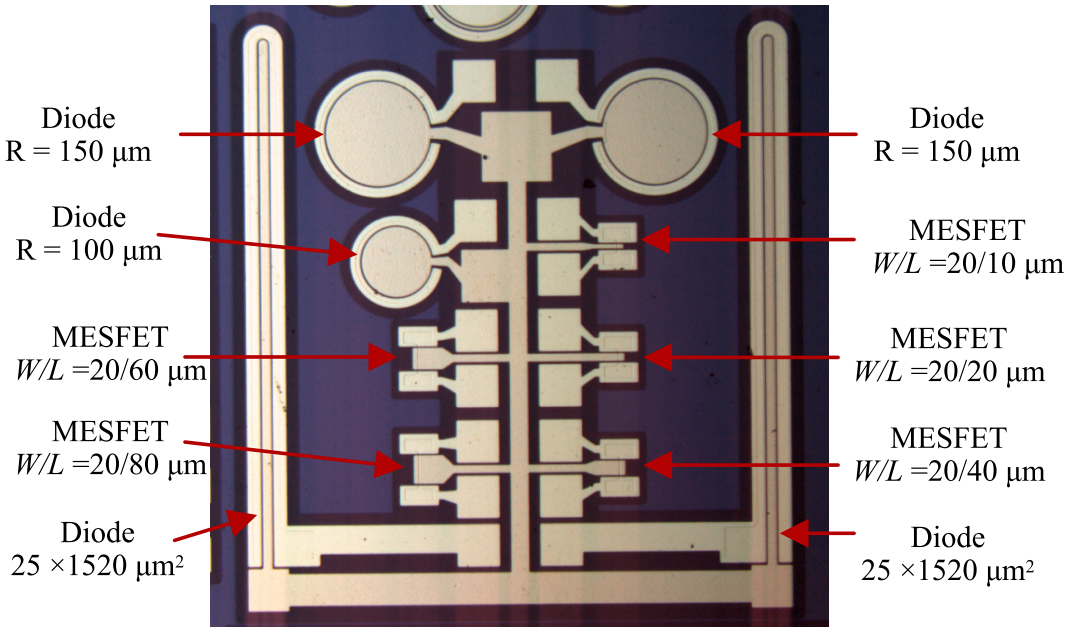


FIGURE 6.21: Central region of microelectronic device chip with transistors and diodes.

The central part of the chip shown in Fig. 6.21 comprises of Schottky diodes and additional transistors. The large circular diodes, each has a diode diameter of 300 μm. Each of the two elongated Schottky diodes has a diode area measuring about 25μm $\times$ 1520 μm. For the transistors located on the central region of the chip, the gate width was kept constant while the gate length increases from 10 μm to 80 μm.

Some test devices incorporated in the device chip other than transistors were used for assessment of device performance. These include the transfer line method (TLM) test structure and a circular Schottky diode with a diameter of 300 μm Schottky in Fig. 6.20. The circular diode was analysed using capacitance-voltage *C-V* measurement to estimate barrier height and donor concentration. The TLM structure consists of ohmic contact pads on the ZnO channel layer with a spacing of 20 μm - 100 μm and is used to determine the contact resistance of ohmic contacts.

It is of note that not all the transistor devices and test structures were used for analyses and assessment of device performance. For each fabricated chip, there is a good number of devices on the chip operational and suitable to confirm transistor behavior and assess performance. For example, MESFET devices with circular geometry shown in bottom right of Fig. 6.19 were excluded for analyses as some of the devices were not operational in the series of fabrications made due to the short-circuiting of terminals.

6.4 Device characterization

In this section, the techniques used for the characterization of the fabricated TFTs are outlined. The transistor characterization performed is based on the standard methods that are used for silicon-based transistors. The two main characteristic parameters for performance assessment of transistor devices are the transfer (I_{SD} vs V_G) and output (I_{SD} vs V_{SD}) characteristics plots. In addition to the drain current, the behavior of the leakage current under gate bias during the extraction of both the output and transfer plots of the transistor can also serve as performance and comparison metrics. Thus, other important transistor performance parameters such as turn-on voltage V_{ON}, threshold voltage V_{TH}, current modulation ratio I_{on}/I_{off}, sub-threshold swing, and channel mobility can be extracted for a TFT. These transistor performance metrics and the results for ZnO based transistor devices are discussed in chapter 7.

6.4.1 Measurement Setup

The measurement of current-voltage (*I-V*) characteristics of devices was carried out using an HP 4155B semiconductor parameter analyzer. The parameter analyzer is equipped with four independent source/measure units (SMU) that can serve as a source of voltage or current and measure the resultant

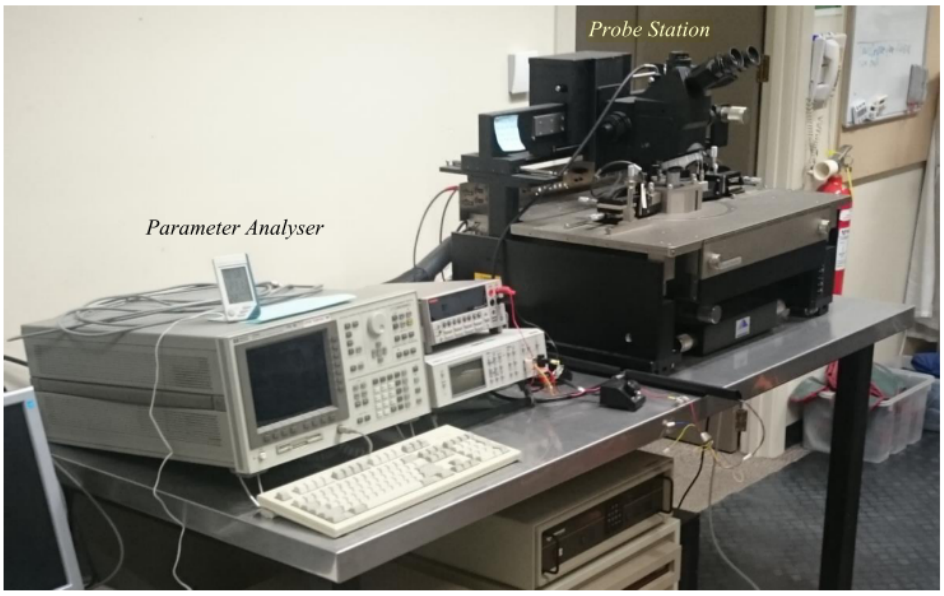


FIGURE 6.22: A Semiconductor parameter analyzer (left) and a probe station used for I-V characterization of fabricated MESFET devices.

current/voltage. Usually, the SMU is set to sweep voltage or current from an initial set point to final value with a specified step size. All sweep input to the parameter analyzer was remotely controlled via an in-house developed control program written in LabVIEW. Output results of measurement are stored as delimited text files which can be plotted and with further data analyses possible.

The HP 4155B parameter analyzer is linked to a probe station with measurement probes attached to the micron range manipulator arm. Under the guidance of a microscope attached to the probe station, the probe tips are placed on the terminals of the device for electrical characterization via inputs from the parameter analyzer.

For temperature-dependent *I-V* measurements, a Temptronic TP03000 system equipped with heating and temperature controller is connected to the stage of the prober. This allows for controlled heating of the sample fixed to the stage with a conductive paste. The maximum temperature achievable by the Temptronic TP03000 is about 140°C. Therefore elevated temperature *I-V* measurements were performed from room temperature up to 130°C.

6.4.2 Capacitance-Voltage Measurement

For the *C-V* measurement of the diodes, a 1 MHz Boonton capacitance meter was connected to the terminals of the probes. Two probes were used to make

electrical contact with the contact electrodes of the Schottky diodes. Voltage bias of 2 V to -2 V was supplied via the parameter analyzer which enables capacitance to be measured with respect to a bias voltage. Measurement of diode capacitance was quantified as analog output from the capacitance meter and sent through the SMU of the parameter analyzer where measurement data is recorded and stored.

6.5 Summary

A metal and n-type semiconductor in an ideal contact behave as either as ohmic contact ($\Phi_m < \Phi_s$) or Schottky barrier ($\Phi_m > \Phi_s$) depending on the work functions of the metal/semiconductor.

A Schottky contact results in upwards band bending and a potential barrier to the flow of electrons from a semiconductor to the metal. A depletion layer is formed in the interface between the metal and semiconductor junction.

An externally applied forward bias voltage reduces the band bending and potential barrier for electrons. Conversely, a reverse bias voltage increases the band bending and the potential barrier.

Fabrication of microelectronic devices such as MESFETs by photolithography using photomasks involve various fabrication steps. For MESFET fabrication, a mask for each photolithographic step was designed for etching/isolation of the channel region, and metallization steps involving deposition of metals or oxidized metal electrodes as ohmic or Schottky contacts.

In the fabrication steps described in the chapter, electron beam evaporation was used to deposit a bi-layer of Ti/Au ohmic contact while RF sputtering was used to deposit thin layers of oxidized metals (e.g. AgO_x) as the Schottky contact.

Device characterization for fabricated MESFETs was primarily done using a semiconductor parameter analyzer connected to a probe station enabling *I-V* characteristics to be performed on devices..

Chapter 7

ZnO-Based MESFETs

7.1 Introduction and Motivation

ZnO is a semiconductor that continues to attract substantial research interest as a material of choice for a range of electronic applications in the optoelectronic industry. Some of its interesting properties include its wide band gap ($\approx$ 3.4 eV), high charge mobility, transparency and ability to undergo deposition and processing at low temperature. Additionally, ZnO is amenable to both wet and dry etching [94], an important property desirable for semiconductor processing techniques for optoelectronic applications. These properties of ZnO make it a potential semiconductor of choice for electronics that are inexpensive but can be of high electronic performance. Some research works are available focussing on ZnO film as the active conducting layer in thin film transistors [142, 58, 51]. As an integral component in modern electronic devices, factors relating to transistor such as performance, reliability, and cost of production need to be considered.

The mist-CVD as a solution processed method for growth of oxide thin films offers some advantages over high and ultra-high vacuum techniques such as PLD and MBE, in that film deposition do not required energy consuming vacuum pump systems. Additionally, the mist-CVD is operated at atmospheric pressure with environmentally friendly precursor salts enabling an economical way of producing ZnO films that can be upscaled for large area and high throughput depositions. Despite the advantages that mist-CVD offers, only a few research works have been reported on mist-CVD deposited films for electronic applications.

In the past decade, oxide semiconductors have drawn the interest of researchers, with a recent incorporation of oxide based thin film transistors (TFT) in commercial display devices [249]. Thin film transistors based on amorphous silicon and polysilicon have dominated the active matrix display

technologies and large area LCD displays for more than three decades. However, the performance of TFT made from amorphous silicon is affected by light sensitivity and degradation in addition to inherent low channel mobility. Even with higher mobilities that can be achieved with polysilicon TFT (between 50 - 500 cm^2/Vs), its opacity limits its use for active matrix display applications. As a transparent oxide semiconductor, ZnO when used as a channel for TFT potentially overcomes some of the shortcomings of silicon based TFT technologies for display [54].

A known problem preventing the full establishment of ZnO based transparent electronics comes from the difficulty in having a reliable and reproducible ZnO of p-type. An option that partly overcomes this limitation is by using a metal-insulator field effect transistor (MISFET) based on ZnO or other related semiconductors. However, MISFETs require a high operating voltage as a result of voltage drop across the insulator-semiconductor junction and suffer from reduced switching speed due to decreased channel mobility from carrier scattering at the interface [60]. Instead, a MESFET with a Schottky junction as the gate rather than an insulator typically offers reduced operating voltage and higher channel mobility compared to MISFET, with charge mobility equal to that of the semiconductor material in the ideal case. For the purpose of quantifying efficiency and performance of a given TFT, figure of merit parameters such as I_{on}/I_{off} ratio, channel mobility, threshold voltage and sub-threshold swing should be within acceptable values. For a transistor to find application in active matrix liquid crystal display (AMLCD), channel mobility of at least 1 $cm^2V^{-1}s^{-1}$ and I_{on}/I_{off} ratio of 10^6 should achieved for large and ultra high definition display technologies [72].

This chapter presents the performance characteristics of MESFET structures fabricated on cheap mist-CVD deposited ZnO films which serve as active conducting channel layer for the transistor devices. Demonstrating excellent transistor characteristics with mist-CVD deposited ZnO films shows the promising potential application of ZnO based electronic devices that are both cheap and also of high performance.

7.2 Results and Discussion

Fabrication of micro-electronic device chips with MESFET structures followed the steps as outlined in chapter 6. All samples of ZnO films used in the MESFET device fabrication were deposited on the r-plane sapphire substrate $(1\bar{1}02)$ at atmospheric pressure using a mist-CVD thin film deposition system

TABLE 7.1: Electrical properties of deposited ZnO film before and after annealing in O_2 atmosphere at 700°C

	As grown	Annealed
Charge concentration, n (cm^{-3})	5×10^{17}	3×10^{17}
Resistivity $\rho(\Omega.cm)$	1.55	1.64
Hall mobility μ_H (cm^2/Vs)	8.0	9.7

as described in chapter 4. A fabricated microelectronic chip contains transistors of various dimensions and geometries in addition to other test structure including diodes and transmission line measurement device (TLM). Electrical characterization of transistor devices was performed according to the experimental procedure described in section 6.4. The discussions of performance characteristics of transistors will first focus on devices fabricated on ZnO film channel with a thickness of approximately 43 nm that utilizes AgO_x as Schottky gate material. Subsequently, a discussion on the effects of channel thickness and gate material on the performance characteristics of transistors is presented.

Table 7.1 shows the electrical properties of as grown ZnO film layer with a thickness of 43 nm before and after annealing which acts as active channel in transistor fabrication. Hall effect measurements at room temperature indicate that as grown ZnO film has charge carrier concentration $n = 3 \times 10^{17} cm^{-3}$, Hall mobility $\mu_H = 9.7\ cm^2V^{-1}s^{-1}$ and resistivity $\rho = 1.6\ \Omega.cm$ after annealing in O_2 atmosphere. As can be deduced from the table, only small changes in carrier concentration, resistivity and mobility were measured post-annealing. The minimal changes after annealing is associated with the relatively small thickness of the channel which makes it more susceptible to effects such as dislocations and strain. In contrast, improvement in charge mobility and increase in film resistivity have been observed for thicker films above 100 nm annealed in oxygen at 700°C. Increase in resistivity post-annealing can be generally attributed to decrease in oxygen vacancies through the adsorption of oxygen at grain boundaries or the evaporation of Zn interstitial after diffusing to the film surface. Increase in charge mobility post-annealing is associated with larger grain sizes and improved film compactness and crystallinity.

As can be seen later in the chapter, the thickness of the active channel layer plays a key role in the performance characteristics of the transistor device. Increased channel thickness has been observed to be associated with

reduced transistor performance parameters such as increased leakage current and decreased I_{on}/I_{off} ratio [248]. The choice of a 43 nm thick film for the initial fabrication of transistor devices was based on available information from the work of Frenzel [58], indicating that relatively thicker films with net carrier concentration approximately 10^{18} cm^{-3} result in degraded transistor performance properties compared with transistors made from ZnO films with thickness less than 50 nm and carrier concentration $\sim 5 \times 10^{17}$ cm^{-3}. Almost all of the subsequent discussions on performance characteristics are for MESFETs fabricated on a 43 nm thick ZnO film layer as active conducting channel using AgO_x as Schottky gate contact. The effect of channel thickness in device performance is presented in section 7.4.

7.2.1 Schottky Barrier Characteristics

The characteristic behaviour of the MESFET is strongly determined by the nature of the gate contact material with a high Schottky barrier desirable for device operation. Since the Schottky diodes crucial in the performance characteristics of MESFETs, the *I-V* characteristics of Schottky diodes integrated in the device chip are analysed.

Figure 7.1 depicts the room temperature *I-V* characteristics plot for two Schottky diodes fabricated on a 43 nm thick ZnO channel with AgO_x as gate material. The diode geometry for one of the diodes is circular with a diameter of 300 μm and the other diode has an elongated gate geometry measuring 25 $\times$1520 μm. These two Schottky diode devices do not serve as gate electrodes for MESFET devices, and hence no drain terminal is part of the structure. In contrast, the *I-V* plot for a source-gate diode that forms a MESFET device defined by gate *W/L* = 100/5 μm is shown in Fig. 7.2.

The conventional thermionic emission theory is used to model current transport through the Schottky gate which assumes that the net current of the device is due to thermionic emission and that parameters such as barrier height and ideality factor are independent of the applied voltage. Based on the thermionic theory outlined in section 6.2.3, the *I-V* relation for a Schottky barrier diode with applied forward bias voltage, neglecting series resistance is given by [8],

$$I = I_0 \left[\exp\left(\frac{qV_a}{\eta k_B T}\right) - 1 \right] \tag{7.1}$$

where V_a is the applied forward bias voltage, η is the ideality factor, T is the temperature and I_0 is the reverse saturation current which can be found from the straight line intercept of $\ln(I)$ vs applied voltage plot shown as inset in

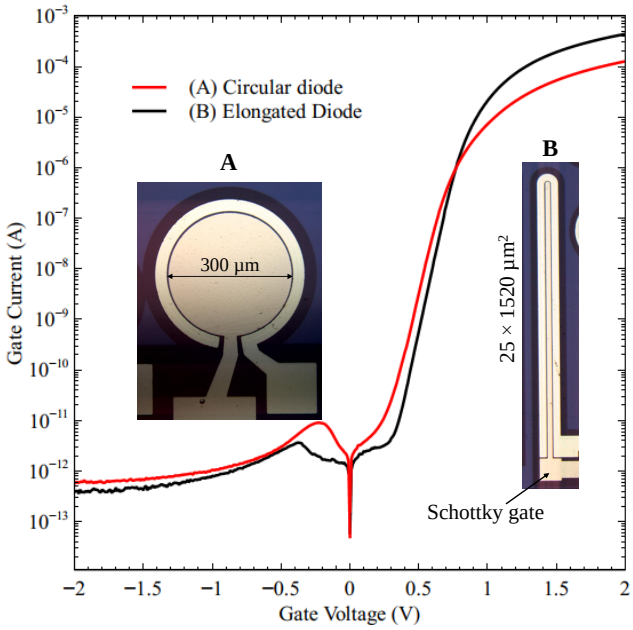


FIGURE 7.1: Schottky diode *I-V* characteristics plots for a circular and elongated gate geometry.

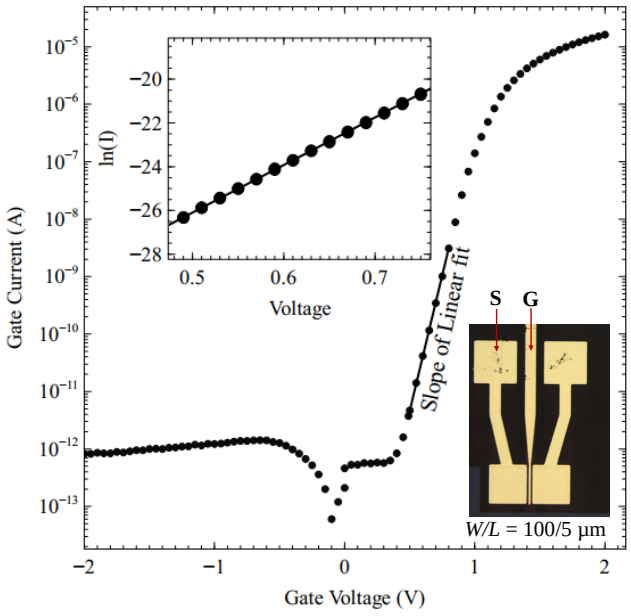


FIGURE 7.2: Schottky diode *I-V* characteristics plot of a source-to-gate contact electrode with diode $L \times W = 5\ \mu\text{m} \times 100\ \mu\text{m}$. Inset graph - plot of $\ln(I)$ vs V_F used to find saturation current.

Fig. 7.2. The reverse saturation current I_0 is given by

$$I_0 = AA^*T^2 \exp\left(-\frac{q\Phi_\text{Bn}}{k_\text{B}T}\right) \tag{7.2}$$

where q is the electron charge, A^* is the effective Richardson's constant taken as 32 A/cm^{2}K^2 for n-type ZnO, T is the temperature in Kelvin, k_B is the Boltzmann's constant and Φ_{Bn} is the effective barrier height at zero bias obtained from Eq. 7.2. For a bias voltage higher than $3kT/q$, the ideality factor η can be obtained from the slope of the linear region of the I-V characteristics curve in semilog axis through the relation

$$\eta = \frac{q}{k_B T} \frac{dV}{d\ln(I)} \tag{7.3}$$

The ideality factor takes into account the difference in the measured I-V characteristics with that of the ideal thermionic emission model. An ideal Schottky diode should have η value of unity. The values of the ideality factor found for the diodes are all higher than unity, typically expected for an ideal diode. Deviation of η from unity can be attributed to the presence of interfacial layers at the AgO_x and ZnO interface, barrier height inhomogeneity or a voltage-dependent image force lowering [251]. The I_0 value was determined to be 8×10^{-17} A. The I_0 value was used to find the Schottky barrier height (SBH) by rearranging Eq. 7.2.

$$q\Phi_B = k_B T \ln\left(\frac{AA^*T^2}{I_0}\right) \tag{7.4}$$

The SBH $q\Phi_{Bn}$ and the ideality factor η found for the elongated Schottky diode as shown in Fig. 7.1 is 1.20 eV and 1.35 respectively. The elongated diode also has a diode rectification ratio (RR) as high as $\sim 10^9$. For the diode with a circular gate, SBH = 1.16 eV and η = 1.43 with RR = $\sim 10^8$. The SBH determined for the source-gate barrier shown in Fig. 7.2 is 1.13 eV with ideality factor $\eta = 1.82$. The slight difference in extracted diode characteristics can be attributed factors that may include inhomogeneous barrier heights, differences in contact area, and variations in contact and series resistance due to differences in geometry.

For a MESFET to be operational with good performance characteristics, a Schottky gate electrode with high barrier is needed. The values of SBH determined for oxidized silver AgO_x as gate contact described are all higher that what is reported for pure Ag metal Schottky diodes. The review by Ozgur *et al*, [173] reports SBH ranging between 0.68 eV - 0.84 eV for pure Ag metal Schottky diodes. The obtained SBH Φ_B between 1.13 - 1.20 eV for the Schottky diodes analysed is comparable to a maximum SBH of 1.20 eV reported

for a AgO_x Schottky diode fabricated on a bulk ZnO wafer [2]. An investigation on Schottky barrier properties and its effect on transistor performance characteristics for other oxidized noble metals is discussed in section 7.5.

7.2.2 Diode *C-V* Measurement

C-V measurement carried out at room temperature was used to estimate the net donor concentration of the channel semiconductor. A relatively large area circular test structure diode with a radius of 150 μm available on the fabricated device chip (micrograph showed on the inset of Fig. 7.1) was chosen to perform the *C-V* analyses. The measurement procedure was performed under forward and reverse bias voltages at 1 MHz frequency as described in section 6.4. A metal-semiconductor junction leads to the formation of a depletion region between the semiconductor and metal materials forming a bias dependent depletion layer capacitance similar to a parallel plate capacitor.

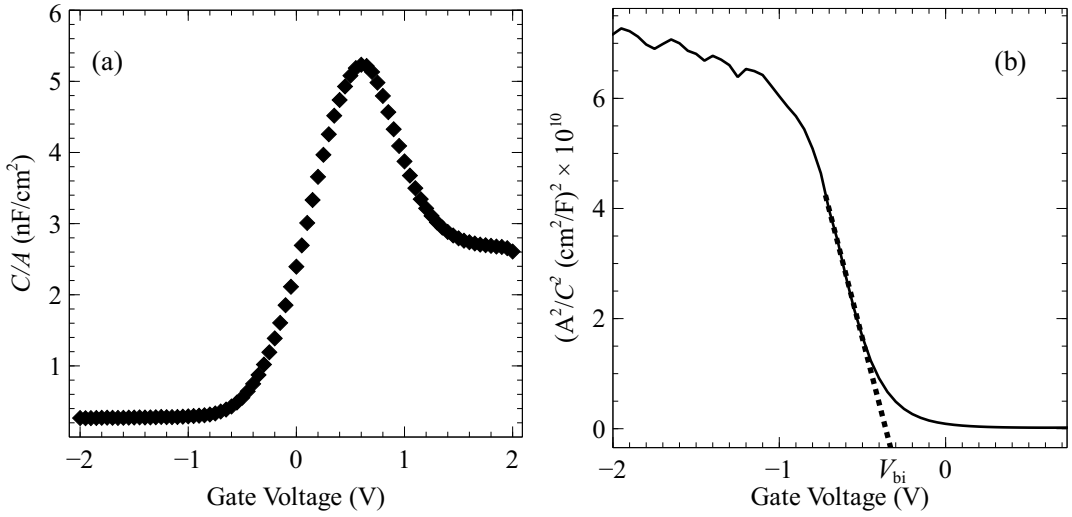


FIGURE 7.3: (a) *C-V* characteristics plot of AgO_x Schottky diode structure fabricated on 43 nm thick ZnO film. (b) A Mott-Schottky analysis plot of $1/C^2$ against bias voltage.

A graph of measured capacitance as a function of bias gate voltage is represented in Fig. 7.3(a). The graph shows that as the reverse bias voltage becomes increasingly negative, the capacitance decreases indicating that the depletion layer thickness increases with reverse bias voltage. The peak in the capacitance is related to charge trapping by interface states and effects of series resistance [233, 110]. For a Schottky diode junction with area A that is under a reverse bias voltage V, the depletion layer capacitance C is given by

[113],

$$\frac{1}{C^2} = \frac{2(V_{\text{bi}} - V)}{A^2 q \epsilon_s N_{\text{D}}} \tag{7.5}$$

where V_{bi} is the built-in potential, ϵ_s is the dielectric constant of the semiconductor, N_{D} is the donor concentration and A is the area of diode.

Mott-Schottky analysis which is a plot of $1/C^2$ against V as shown in Fig. 7.3(b) is a commonly used method for finding donor concentration and built-in potential V_{bi} from the slope and intercept with the voltage axis. The slope of the graph is used to determine the N_{D} to be $1.4 \times 10^{18}\text{cm}^{-3}$. To obtain V_{bi} an anomalous behavior is observed in which the extrapolated intercept with the voltage axis gives a negative built-in potential. An explanation is based on the fact that the overall Mott-Schottky capacitance analysis relies on the depletion approximation which assumes that there are no free carriers in the depletion region. For a very thin film layer where the thickness of the depletion layer is comparable to the film thickness, the depletion layer approximation is no longer valid and leads to erroneous results in both the built-in potential and donor concentration [125]. Further, for a material with low donor density, effects of chemical capacitance (also called diffusion capacitance) that describe measured capacitance being dominated by charge carriers injected from the metal contact instead of charges from the donor atoms lead to misinterpretation of *C-V* measurements [113].

As noted by Ref. [113], the use of Mott-Schottky analyses for thin films of 100 nm and below, with low donor concentrations can lead to erroneous results. In particular, the violation of depletion approximation can lead to a strong underestimation of built-in potential. Based on these, the interpretation of such *C-V* analyses should be done with care. Other considerations to be made on interpretation of *C-V* analyses include systematic errors associated with instrument problems such and parasitic inductance originating from the measurement leads, that degrade accuracy of measured capacitance. Also, there is frequency dependence on measured capacitance, with higher capacitance typically measured at low-frequency [121].

7.3 Transistor Performance

In this section, results and assessment of performance parameters for transistors are discussed in relation to the electrical measurements done on microelectronic transistors fabricated on a 43 nm thick ZnO film sample using

AgO_x as Schottky gate. The key aspects of transistor performance are generally assessed from the output and transfer characteristics plots. Some other performance measures such as transconductance, channel mobility and subthreshold slope are derived from these plots.

7.3.1 Output and Transfer Characteristics

The microelectronic device chip has several transistor test structures which are used to characterize the effect that variations of the transistor geometric design can have on the performance characteristics. Two important performance metrics for characterizing a transistor device are the output and transfer plots. The output characteristics is a plot of source-drain current I_{SD} as a function of source-drain voltage V_{SD} for different gate voltages V_G. The transfer characteristic curve is a plot of source-drain current I_{SD} against varying gate voltages V_G at a constant source-drain voltage V_{SD}. The output and corresponding transfer characteristics of a MESFET device defined by W/L = 100/5 μm, plotted on linear scale of I_{SD} axis is shown in Fig. 7.4. For the output plot, the source-drain voltage V_{SD} was varied from 0 - 3V while the gate voltage was increasingly reverse biased starting from V_G = 1 V with a step of -100 mV to V_G = - 0.4 V. The transfer characteristics plot was acquired by maintaining V_{SD} constant at 3 V, ensuring saturation of the channel, while the gate voltage is increasingly reverse biased starting from V_G = 2 V.

The characteristic curves depicted in Fig. 7.4 is clearly a textbook example of a field effect transistor behaviour with a clear pinch-off and saturation of the drain current modulated by the gate voltage V_G. The output curve shows that when the applied V_{SD} is small, the drain current is linear with the applied voltage (ohmic region). As the V_{SD} increases further, saturation of the drain current occurs at the pinch-off point beyond which further increase in V_{SD}, do not result to a substantial change in the drain current. The drain current in the saturation region is dependent on the gate voltage V_G, increasing in value for higher gate voltage. The linear scale transfer characteristics plot show very low drain current below a threshold gate voltage and an almost linear increase of drain current above the threshold gate voltage. The transfer plot in linear scale allows for the extraction of threshold voltage of a transistor device.

Further transistor performance metrics can be derived from the transfer characteristic plotted on a logarithmic scale. This is shown in Fig. 7.5 which graphs transfer characteristics of transistors defined with a constant

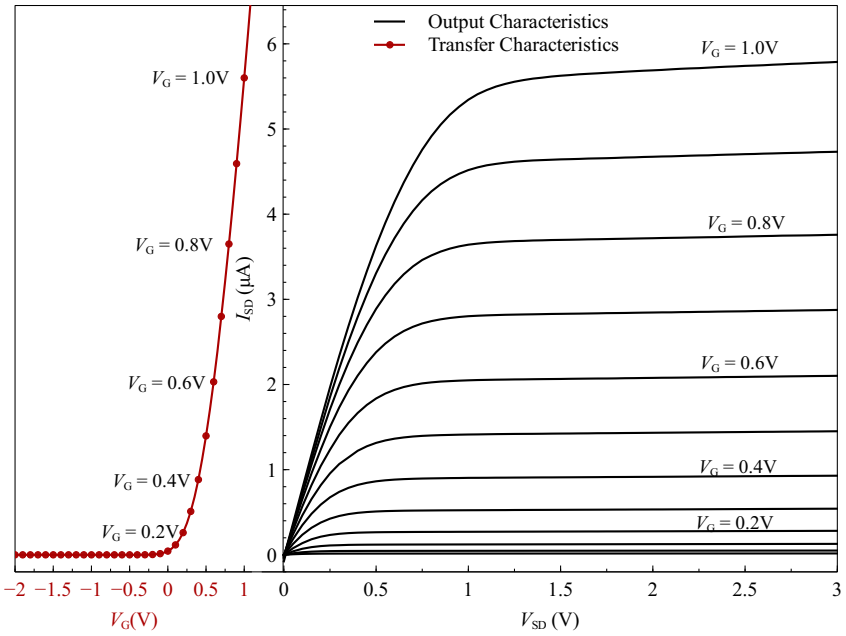


FIGURE 7.4: Linear scale output and transfer characteristic plots of a transistor defined by gate W/L = 100/5 μm fabricated on a 43 nm thick ZnO film with AgO_x as Schottky gate.

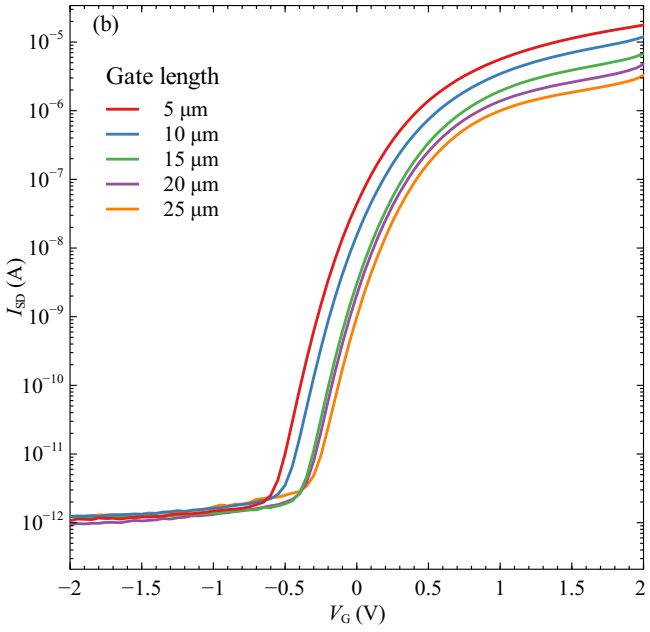


FIGURE 7.5: Logarithmic-scale transfer characteristics plots of MESFET structures with a gate width W = 100 μm and varying gate lengths, L = 5μm - 25 μm.

gate width W = 100 μm, but with increasing gate length from L = 5 μm - 25 μm on a logarithmic scale. Transfer plot in logarithmic scale allows for improved assessment and observation of effects on the drain current due to gate voltage. As the gate voltage becomes more reverse biased, the drain

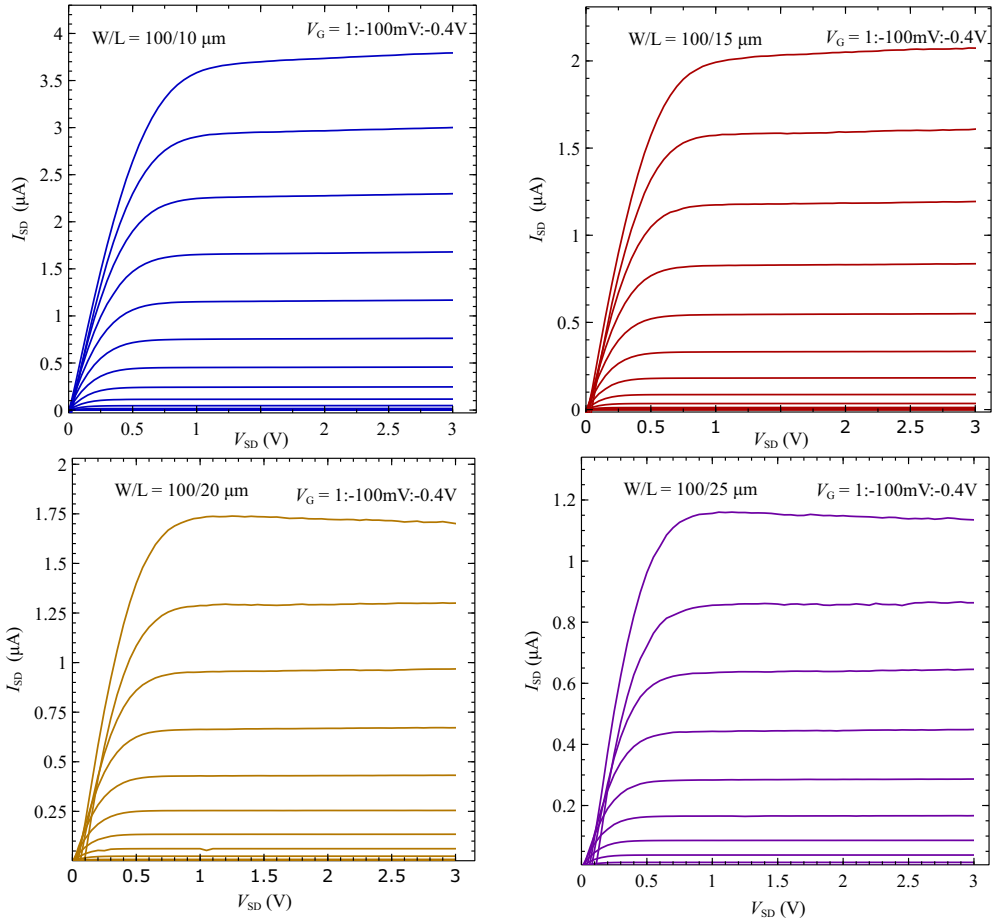


FIGURE 7.6: Output characteristic plots for MESFETS structures with gate width W = 100 μm and varying gate length L = 10μ - 25μm.

current continuously decreases due to the widening of the depletion layer. With further negative biasing of the gate, the channel is completely depleted leading to the cut-off of the current to the drain. The reverse leakage current was found to be in the range of pico-amperes. The transistor I_{on}/I_{off} current ratio(current modulation ratio) of 1.7 $\times 10^7$ was found for a MESFET device with gate W/L = 100/5μm.

It can be deduced from the transfer plots in Fig. 7.5 that maximum on-state drain current measured at V_G = 2 V decreases as the gate length is increased at a fixed gate width. The I_{on}/I_{off} ratio reduced by an order of magnitude from approximately 10^7 to 10^6 with gate length increase from 5 μm to 25 μm. The reverse leakage current was not observed to substantially change with increased gate length. As the length of the gate increases, the area of the field effect charge cloud when a gate voltage is applied enlarges thereby

increasing current resistance from the source to the drain. The output characteristic plots for other transistor structures on the device chip defined with a constant gate width W = 100 μm with varying gate lengths from 10μm - 25 μm is shown in Fig. 7.6. These graphs generally depict increase in transistor output drain current for reduced gate length. All of the transistors show field-effect induced drain current saturation and pinch-off that is modulated by the gate voltage.

To investigate the effect of gate width-to-length ratio (W/L) on the drain current of MESFETs, two different arrays of MESFETs fingers fabricated on the chip were chosen for the analyses. The first array, tagged Array(A) in Fig. 7.8 contains 10 transistor devices with a common gate terminal, and fabricated on a continuous ZnO channel layer (all devices not shown on the micrograph). Five transistors in the array have a fixed gate length L = 5 μm, with gate width varying from 10 μm to 50 μm. The five other transistors have a constant gate width of W = 50 μm but with variation in gate length from 5μm to 25 μm. This array was used to determine drain current at gate W/L ratio ranging from 2 to 10.

The transfer characteristics of all the transistor structures in Array(A) is plotted in Fig. 7.7. Transfer plots for fixed gate width W as depicted in the graph of Fig. 7.7(a) show a decrease in the on-state drain current as the gate length increases. Conversely, transfer curves in Fig. 7.7(b) show that on-state drain current increases for larger gate width at a fixed length. This trend is in line with field effect transistor characteristics which based on Eq. 6.19, the conductance through the transistor channel is directly proportional to its width-to-length ratio (W/L).

Similar to the array described above, another set of transistors tagged as array(B) as shown in Fig. 7.8 contains devices, also fabricated on a continuous ZnO film as channel layer. The transistor structures each has a gate width, W = 200 μm but with varying gate length L = 5 - 25 μm. This array enabled the assessment of transistor drain current for gate W/L ratio varying from 8 - 40.

The variation of the drain current in the saturation region measured at source-drain voltage V_{SD} = 3 V and a gate voltage V_G = 2 V is represented in Fig. 7.8. As expected of field effect transistor devices, the channel conductivity for both arrays measured through the drain current is proportional to the W/L ratio of the device. The linear relationship between the drain current and the W/L ratio of the transistor is consistent with Eq. 6.25, indicating direct proportionality between drain current and gate W/L ratio when other

variables are kept constant.

An interesting observation from the plot shows that for the two arrays where W/L is equal to 8 and 10, the drain current was higher in array B than in array A. This somewhat appears to be anomalous considering that MESFET array(B) has ZnO film layer with a width of 200 μm compared to the maximum channel width of 50 μm for array(A). Thus, without considering

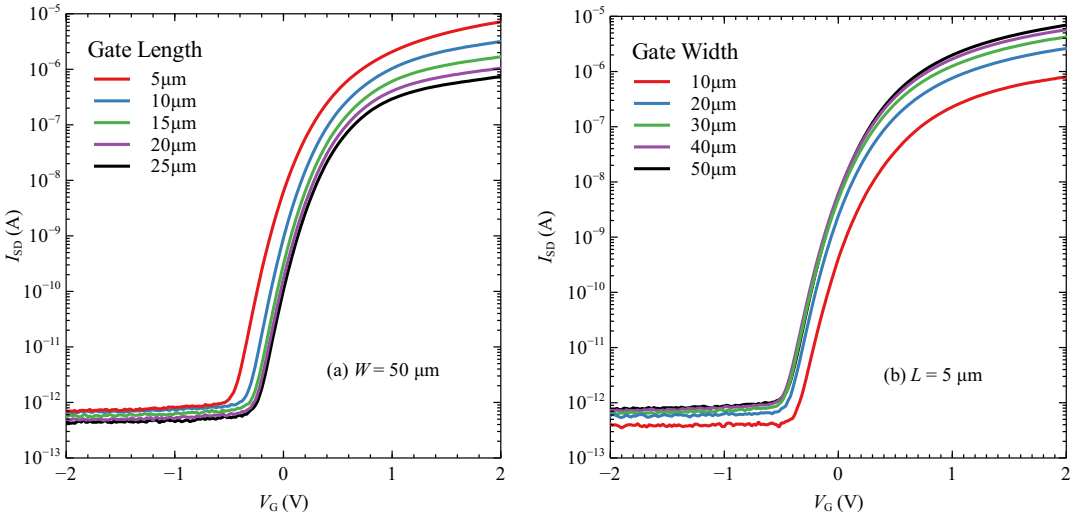


FIGURE 7.7: Transfer plots for MESFETs fabricated on a 43 nm thick ZnO with (a) W = 50 μm, and L varying from 5 μm to 25 μm (b) L = 5 μm, and W varies from 10 μm to 50 μm.

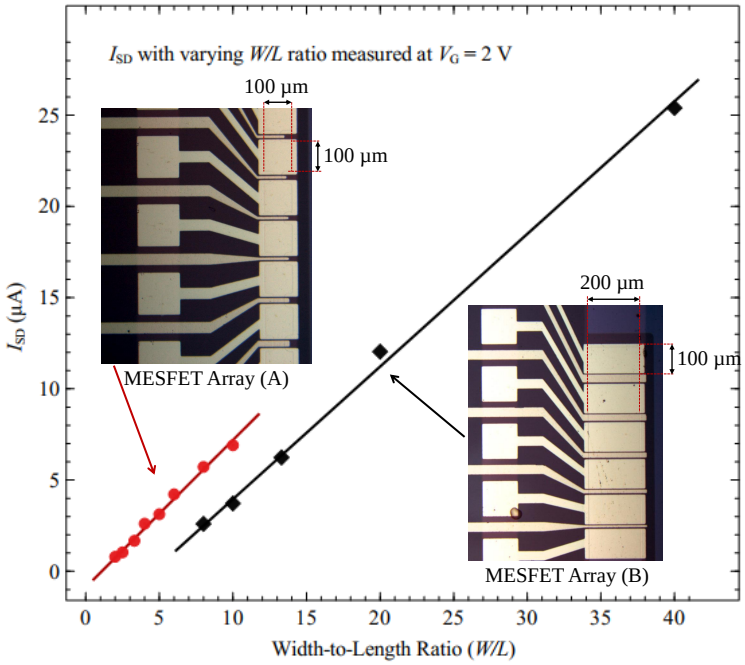


FIGURE 7.8: Variation of drain current as a function of gate W/L ratio for arrays of MESFETs.

other factors, the current should be higher for the channel with larger width and lower resistance. An explanation for the increased current for a channel layer with higher resistance is based on the varying area of the Schottky gate. Since the gate electrode controls the channel opening, the contact area for the gate electrode in MESFET array(B) is higher, and thus restricts current more effectively than in array(B), even for transistors with the same *W/L* ratio.

7.3.2 Threshold Voltage/Turn-On Voltage

The threshold voltage V_{TH} determines the value of the gate voltage above which the transistor begins to conduct and is typically extracted from the transfer characteristics plot. For an n-channel enhancement mode FET, current conduction through the channel is not established without a positive gate bias voltage, turning on the transistor. Conversely, a depletion mode FET has a conductive channel that exists naturally thus, V_{TH} does not necessarily correspond to a turn on voltage for depletion devices but ambiguously indicates a gate voltage at which the channel is wide enough to enable electrons to flow unrestricted. Several extraction methods are employed to determine the threshold voltage V_{TH} of a transistor [170], with obtained values that are dependent on the method used. Particularly for micro-electronic transistor devices, short channel effects such as drain induced barrier lowering (DIBL) play a part to further create ambiguity in the extracted V_{TH} . Likewise, V_{TH} is affected by several device parameters such as gate width, gate overlap, gate length and temperature [208].

TABLE 7.2: Threshold voltage/Turn-on voltage for MESFETs of varying gate lengths.

Length (μm)	V_{TH}[†] (mV)	V_{TH} [§] (mV)	V_{ON} (mV)
5	2	29	-477
10	59	101	-380
15	135	188	-327
20	125	147	-256
25	146	207	-207

[†] V_{TH} derived from extrapolating of $\sqrt{I_{SD}}$ vs V_G plot.
[§] V_{TH} extrapolated from linear region of transconductance plot.

A method for V_{TH} extraction that involves the extrapolation of the linear region of $\sqrt{I_{SD}}$ vs V_G plot is widely used in MOSFETs and MISFETs. This method assumes a square law relationship between the drain current and

the gate voltage in the saturation region, hence V_{TH} can be extracted by plotting $\sqrt{I_{SD}}$ against V_G. This extraction method was applied to estimate the threshold voltage of fabricated MESFET devices and is depicted in Fig. 7.9. Another extraction method proposed by [217] derives V_{TH} by extrapolating the linear part in the plot of transconductance vs. gate voltage (see Fig. 7.10). Additionally, V_{TH} can be extracted by simply extrapolating the linear part of the transfer plot to zero gate voltage for channels that are not in pinch-off state. These methods are inherently affected by the choice of data points in the linear region and dependent on the assumptions of the models. It is often typical for transistor devices to deviate from the assumed ideal behaviour underlying the extraction method.

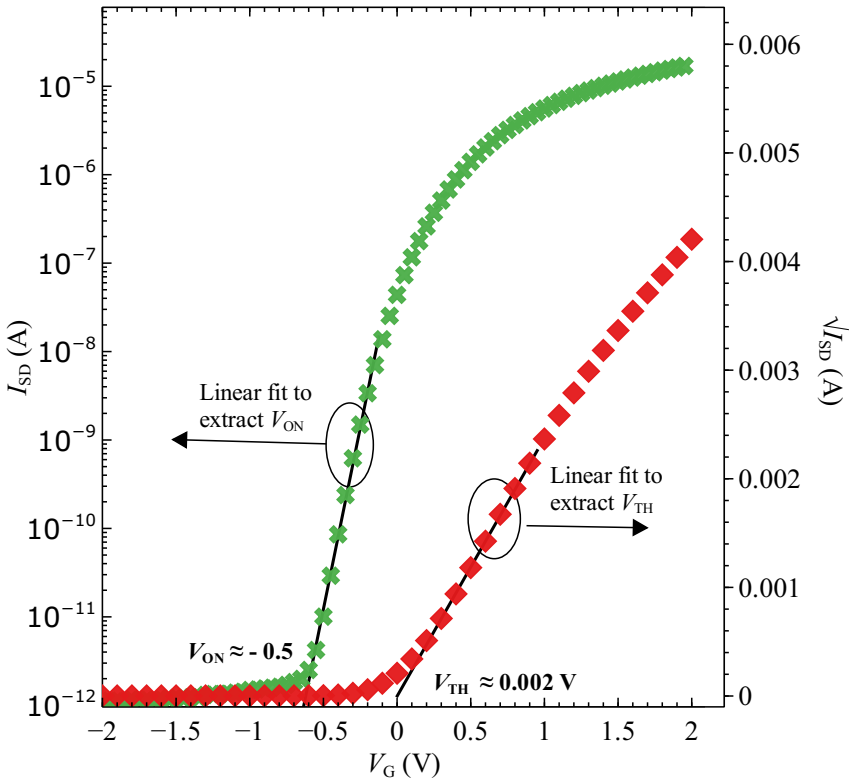


FIGURE 7.9: Extraction of threshold voltage V_{TH} and turn-on voltage V_{ON} for MESFET structure with W/L = 100/5 μm.

A more preferred assessment parameter is the turn-on voltage V_{ON} which reduces the ambiguity and variabilities based on the extraction method used. The V_{ON} is simply defined as the gate voltage at which the drain current starts to substantially increase as seen in the $\log(I_{SD})$ vs. V_G graph. The graph in Fig. 7.9 shows a method of finding V_{TH} by extrapolating the linear region of $\sqrt{I_{SD}}$ vs. V_G plot in addition to extracting V_{ON} from a plot of $\log(I_{SD})$ vs. V_G. Further, as can be observed on Table 7.2 which shows V_{TH} and V_{ON}

for transistor structures with defined gate width of 100 μm but with varying gate lengths, the V_{TH} value determined by two different methods gave varying results. One may even classify these devices as enhancement mode transistors based on their V_{TH} value. However, V_{ON} shows that negative cut-off gate voltage is required to deplete the channel implying that these devices are normally on at zero bias gate voltage and therefore considered depletion mode transistors.

7.3.3 Transconductance

The transconductance usually symbolized as g_m with unit Siemens (S) is used to determine the current operating region for the transistor device obtained as a ratio of the change in drain current with respect to the gate voltage $\frac{dI_{SD}}{dV_G}$ at a constant V_{SD}. The gain of a transistor device is constrained by the transconductance. The use of transconductance is however, of limited use for wide comparisons of transistors fabricated on different materials and geometries since transconductance is dependent on the physical size of the device.

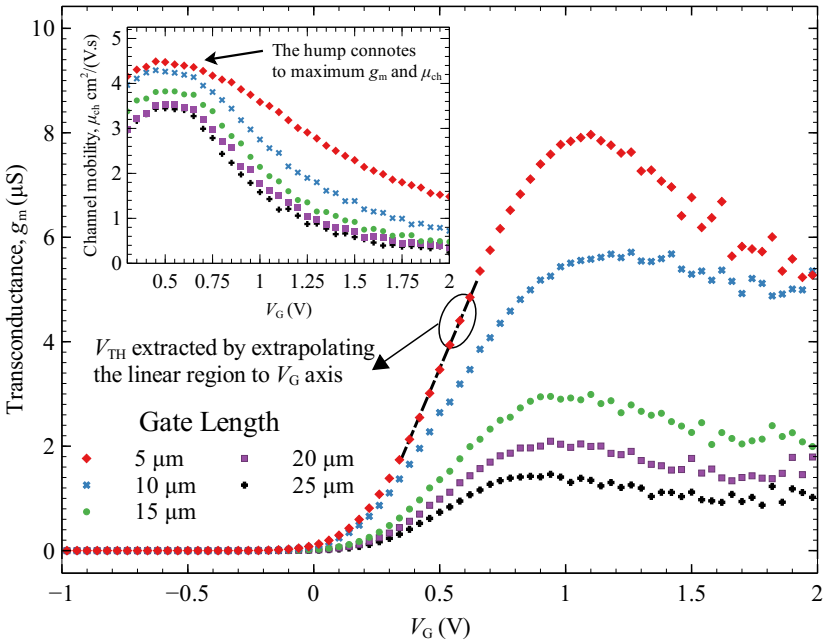


FIGURE 7.10: Transconductance plot for MESFET structures with a gate width of 100 μm, with varying gate lengths. Inset - The transconductance is used to estimate the channel mobility using Eq. 7.7.

The transconductance plot for MESFETs with gate width of 100μm, and varying gate length from 5μm to 25μm is shown in Fig. 7.10. As expected

based on theory of FETs and physical meanings of Eqs. 6.19, the transconductance inversely varies with the channel length. The point of maximum transconductance occurs approximately at a gate voltage of 1.0 V. For a gate length increase from 5 μm to 10 μm, a change in g_m is from about 8μS to 5.5μS corresponding to a percentage difference of 45%. This change in transconductance consistent is with simulation studies on field effect transistors reported in the literature [155]. A higher value of transconductance implies that the gate has a better control of the channel which potentially leads to improved current gain and high frequency capabilities [154].

7.3.4 Channel mobility

The channel mobility indicates the ease at which charge carriers move through the device and is one of the most important device performance metrics. The channel mobility is affected by the method of fabrication, semiconductor material, lattice vibration, grain boundaries, impurities, and defects [155, 182]. The intrinsic mobility of the ZnO film semiconductor material serving as the active channel is obtained from Hall measurement. However, in a TFT device, it is typical for the mobility to deviate from that of the film material. The mobility of charge carriers are reduced by scattering from the interface of the M-S junction.

The channel mobility given in Eq. 6.19 based on the theoretical background outlined in chapter 6 is written as

$$\mu_{ch} = \frac{g_0 L}{q N_D h W} \tag{7.6}$$

where g_0 and N_D are the maximum transconductance and donor density respectively, h is the channel thickness while L, W represent the length and width of the gate. However, finding the channel mobility using the above equation is very sensitive to the value of N_D with an estimated result that can be largely inaccurate especially with low donor concentration and small thickness of film below 60 nm. For very thin films, channel depletion is fast over a short range of bias voltage. The channel mobility can be extracted alternatively using the maximum saturation region transconductance g_m expressed as [52],

$$\mu_{ch} = \frac{g_0 h L}{\epsilon_s (V_G - V_{TH}) W} \tag{7.7}$$

where g_0 is the maximum transconductance determined from the transfer characteristics plot of the MESFET, h is the thickness of the channel while

V_{TH} is the threshold voltage determined by the linear extrapolation of $\sqrt{I_{SD}}$ vs. V_G as shown in Fig. 7.9. The dielectric constant ϵ_s is taken as 8.5 for ZnO.

A plot of channel mobility calculated from Eq. 7.7 is shown in the inset of Fig. 7.10. The hump in the plot estimates the maximum channel mobility which corresponds to the V_G that gives the maximum transconductance across the device. The plot depicts a decrease in μ_{ch} with increase in the gate length of the transistor devices. It shows that mobility of the carriers is dependent on the gate voltage V_G with maximum mobility corresponding to about the same gate voltage that yields the maximum transconductance. An estimated maximum channel mobility extracted for a device with L = 5 μm is about 4.3 $cm^2/(V.s)$ while for L = 25 μm, mobility was found to be 3.5 $cm^2/(V.s)$. Increased channel mobility for shorter gates is associated with fewer traps in the grain boundary at decreased gate lengths [155]. Additionally, the drain current is a product of width-to-length ratio W/L and mobility, hence a decrease in gate length results in an apparent increase in the mobility [83].

The channel mobility μ_{ch} is about half the value of carrier mobility μ_H of the underlying ZnO film channel, derived from Hall measurement. It is desirable and a key merit of MESFETs as opposed to MISFETs, for the channel mobility of the device to match that of the underlying semiconductor material. However, a reduction in the mobility of carriers in the fabricated device is associated with the M-S interface which provides means of charge scattering and reduces mobility of charge carrier through the channel.

7.3.5 Sub-threshold Slope

The sub-threshold slope S quantifies the switching ability of the transistor and corresponds to the value of gate voltage V_G that will increase/decrease the I_{SD} by one decade. The sub-threshold slope is related to the density of surface trap states in the semiconductor band gap [246]. The S value is extracted from the transfer characteristic plot of $\log(I_{SD})$ vs V_G plot by taking the slope of linear data points in the sub-threshold region. It is given by the equation [246],

$$S = \frac{dV_G}{d(\log_{10} I_{SD})} \tag{7.8}$$

The extracted S value was 118 mV/decade for a MESFET structure defined by channel W/L = 100/5 μm of with S obtained for other MESFETs structures ranging between 116 - 125 mV/decade depending on the selected data points used for the linear fit. This is in agreement with numerical simulation

studies on FET reported by Mittal *et al*, [155] where the sub-threshold slope varies slightly and shows an almost constant behaviour for top and bottom gate transistor devices with gate lengths from 5μm - 40 μm. It is desirable to have a low value of S since a smaller value implies that a smaller change in gate voltage is required to turn the transistor from off-state to on-state and thus, less power consumption. In addition to a V_{TH} value as close to 0 V as possible, a sub-threshold slope of <100 mV/decade is desirable in order to reduce power consumption and operating voltage of the device [182]. The switching capacity quantified through our sub-threshold slope for the fabricated transistors is substantially lower than ~600 mV/decade obtainable in a-Si MOSFET devices [130].

7.3.6 Contact Resistance Analyses

Another parameter that affects the performance of TFT devices is the contact resistance. The quality of connection made by the source/drain electrodes on the active semiconductor layer plays a role in the transistor operation. On the source and drain contacts, it is desirable to have an ideal ohmic contact with very low contact resistance - i.e. source/drain contacts with no barriers such that current flows irrespective of the polarity of the voltage.

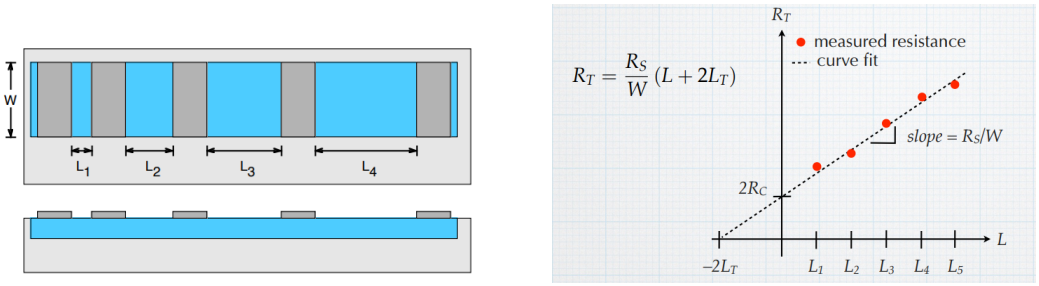


FIGURE 7.11: Illustration of how a TLM structure comprising of ohmic contacts with varying spacing is used to extract R_s, R_c and L_T.

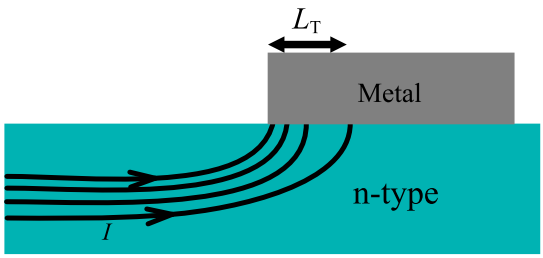


FIGURE 7.12: Current crowding at the edge of a contact. There is an exponential drop in current away from the edge

An ohmic M-S interface can have a linear *I-V* characteristics behaviour but with either a low or high contact resistance. Conversely, it can also be non-ohmic and with a low or high contact resistance. When an ohmic contact has a high contact resistance, it induces a voltage drop at the source/drain contacts which influences the electrical performance of the device. For TFTs with a short channel, the gate length may be so small that the contact resistance dominates that of the channel resistance, making the electrical characteristics susceptible to the contact resistance. Some of the effect of high contact resistance may include worsening of transconductance and reduction of carrier mobility [46]. The resistance measured on a semiconductor channel with two ohmic contact pads consists of contributions from the metal contact, the semiconductor channel and the metal-semiconductor interface. Since the resistance of the metal contact is low compared to the interface, the resistance of the metal is typically ignored for analyses of contact resistance. The total resistance R_T measured for a channel layer with ohmic M-S contacts is therefore given by,

$$R_T = R_s \frac{L}{W} + 2R_c \tag{7.9}$$

where R_s is the sheet resistance of the semiconductor, L and W represent the length and width of the semiconductor channel and R_c is the contact resistance associated with the M-S interface.

A transmission line measurement (TLM), also called transfer length measurement consists of ohmic contacts with varying channel spacing which is employed to assess the quality of ohmic contacts. The TLM enables three parameters to be extracted based on the theoretical background illustrated in Fig. 7.11. The slope of a plot of total resistance R_T against channel spacings is used to find the sheet resistance R_s if the contact width W is known. The intercept at $L = 0$ is $R_T = 2R_c$ gives the contact resistance. The intercept at $R_T = 0$ is used to find the contact resistivity ρ_c. For comparison purposes, specific contact resistivity ρ_c is a more preferred parameter since unlike contact resistance, it is not dependent on the size of the contact. The relationship between specific contact resistivity ρ_c and contact resistance R_c is given by

$$\rho_c = R_c A_{eff} \tag{7.10}$$

where A_{eff} is the effective contact area responsible for current injection.

To better understand the concept of contact resistivity, diagram in Fig. 7.12 shows a metal contacted on top of a semiconductor. The flow of current

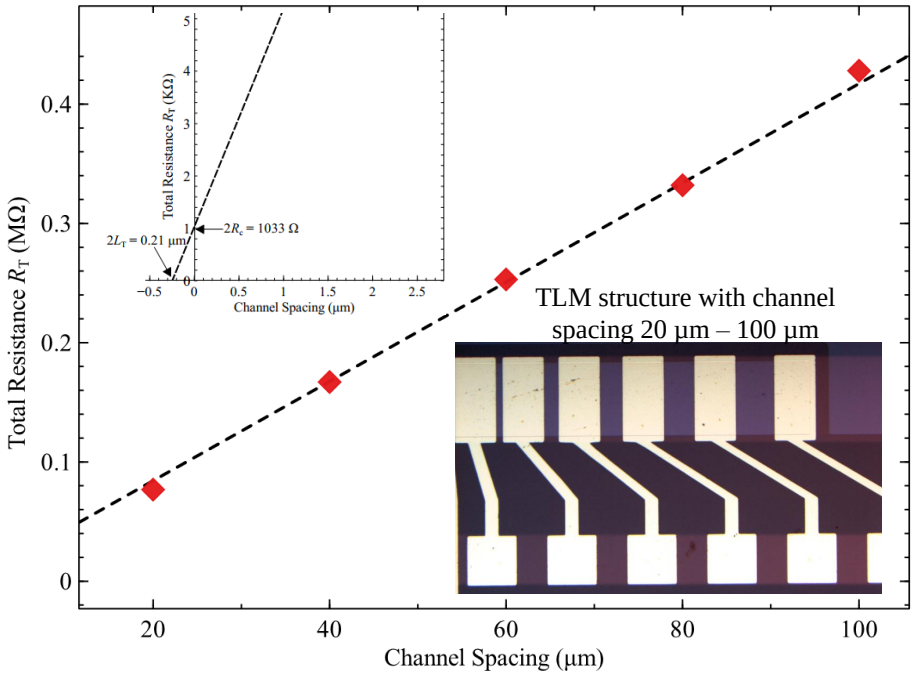


FIGURE 7.13: A plot of total resistance for different channel spacings for a bi-layer of Ti/Au ohmic contact on ZnO film as channel. Inset plot - focussed linear fit line extrapolated to zero channel spacing for finding ρ_c and L_T.

to the metal is not uniform, with distribution of the current density dependent on the contact resistivity ρ_c. When ρ_c of the metal is small, the current flows quickly into the metal using the edge of the contact area of the metal for conduction. For higher ρ_c, the current conduction spread through a larger area of the contact. At the edge of the contact, the current flow in and out of the metal contact is quite significant but drops off until at the far edge, there is no current. This phenomenon is termed "current crowding". Current crowding across the contact drops off exponentially with a characteristic length known as the transfer length. The transfer length of the contact signifies the length at which the voltage drops to $1/e$ of its original value. The transfer length is the average distance the charge carrier travels in the semiconductor beneath the contact before it flows into the contact. The transfer length L_T is given as

$$L_T = \sqrt{\frac{\rho_c}{R_s}} \tag{7.11}$$

Eq. 7.10 can then be written in the form by substituting for A_{eff}

$$\rho_c = R_c W L_T \tag{7.12}$$

$$R_c = \frac{R_s L_T}{W} \tag{7.13}$$

The total resistance R_T can then be expressed as

$$R_T = \frac{R_s L}{W} + \frac{R_s}{W} 2L_T \tag{7.14}$$

By extrapolating to $R_T = 0$, L_T is found which is used to find specific contact resistivity using Eq. 7.12.

A TLM test structure with contacts of spacings ranging from 20 μm to 100 μm available in the device chip and shown as inset micrograph in Fig. 7.13 is used to estimate contact resistance of an ohmic contacts. For each channel spacing on the TLM structure, a voltage of 0 - 2 V was passed through and the current measured. The slope of the *I-V* plot was used to determine the total resistance R_T according to Ohm's law. A plot of total resistance against channel spacing is shown in Fig. 7.13. A linear regression line was fitted to the plot which confirms the linear relationship between voltage and current for the Ti/Au ohmic contacts.

The inset plot in Fig. 7.13 is a zoomed-in plot of line fit extrapolated to the intercept on the x-axis and y-axis. The value of the contact resistance R_c obtained for the bi-layer of Ti/Au contact is 517 Ω while transfer length L_T = 0.21 μm. The contact resistivity is found to be ρ_s = 3.67 $\times 10^{-4}$ Ω-cm. This value is similar the value of 1 $\times 10^{-4}$ reported for Ti/Au ohmic contact on epitaxial ZnO thin film [78]. Other values of contact resistivity reported for Ti/Au contact on ZnO include 1.5$\times 10^{-5}$ Ω-cm (n = 3$\times 10^{18}$) [109] and 4.8 $\times 10^{-5}$ Ω-cm [158].

The TLM method has some drawbacks in terms of accuracy of extracted values. The method assumes that the sheet resistance under the contact is equal to the semiconductor sheet resistance. Further, it also assumes a constant electrical and geometrical contact parameters across the sample. However, such parameters are known to exhibit scatter across a sample.

7.4 Effect of active layer thickness

The thickness of the channel layer is very vital in the performance characteristics of MESFET devices and has been shown to influence film surface

morphology and also transistor performance characteristics including channel mobility, I_{on}/I_{off} ratio and threshold/turn-on voltage [248].

To investigate the effects of channel layer thickness on the performance characteristics of MESFET devices, two additional chips were fabricated on ZnO film samples with different thicknesses. The thickness of one of the samples is 30 nm, which is less than the previously discussed MESFET device. Additionally, another device chip was fabricated on a film with thickness of 65 nm. The fabrication process including the choice of ohmic metals and Schottky gate material (i.e. AgO_x) is similar to that of the 43 nm thick channel layer discussed so far.

For the ZnO film channel with thickness of 65 nm, charge carrier concentration n of an as-grown film obtained from Hall effect measurement is 1.3 $\times 10^{18}$ cm^{-3} while Hall mobility μ_H = 9.1$\pm$1.0 cm^2/V.s and resistivity ρ = 3.4 $\times 10^{-1}$ Ω-cm. Annealing in O_2 at 700°C reduced n to 7.6 $\times 10^{17}$ cm^{-3}. Similar to ZnO film channel layer with a thickness of 43 nm, no substantial changes in the mobility and resistivity were measured after annealing, most likely due to the small thickness of these samples. For the other ZnO film sample that is 30 nm thick, a consistent and reliable Hall measurement could not be obtained as the film conductivity was very low beyond the limit of measurement by the Hall instrument. It is estimated that charge carrier concentration n for this film sample will be $\approx 10^{16}$ cm^3.

The comparisons of various transistor performance characteristics for the different thickness of channel layers are shown in Figs. 7.14 and 7.15. These comparisons are made on a MESFET structure defined by W/L = 100/5 μm but with channel thickness of 30 nm, 43 nm and 65 nm. It is shown that the drain current (at V_G = 2 V) is highest for the thickest channel layer with I_{SD} found to be 146 μA, 17 μA and 3 μA for channel thicknesses of 65 nm, 43 nm and 30 nm respectively. The transconductance plot follows a similar trend on channel thickness dependence with maximum transconductance obtained for the thickest channel layer.

The transfer characteristics plots for different channel thicknesses is shown in Fig. 7.14(a). The turn-on voltage is shifted towards increased negative gate voltage with increase in channel thickness. The turn-on voltage V_{ON} for the 30nm, 43nm and 65 nm channel layers are estimated to be -0.30 V, -0.6 V and -3.6 V respectively. The extracted V_{ON} values were all negative and increase in absolute value as the thickness of the channel layer is increased. A large negative turn-on or threshold voltage is associated with the relatively large number of free charge carrier concentration of the ZnO thin film active

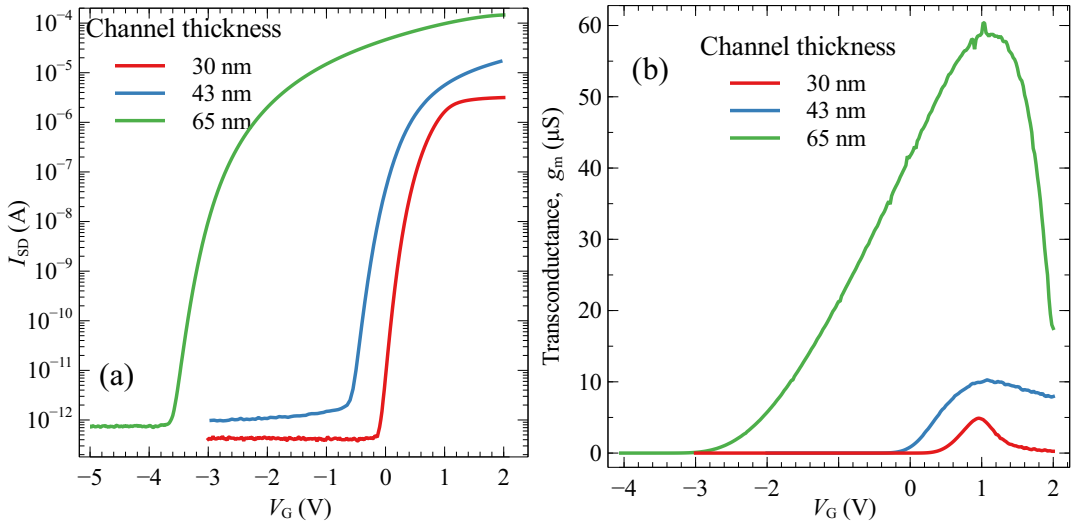


FIGURE 7.14: (a)Transfer characteristics plots and (b) Transconductance plots for MESFETs defined by channel W/L = 100/5 μm fabricated on ZnO films of different thicknesses.

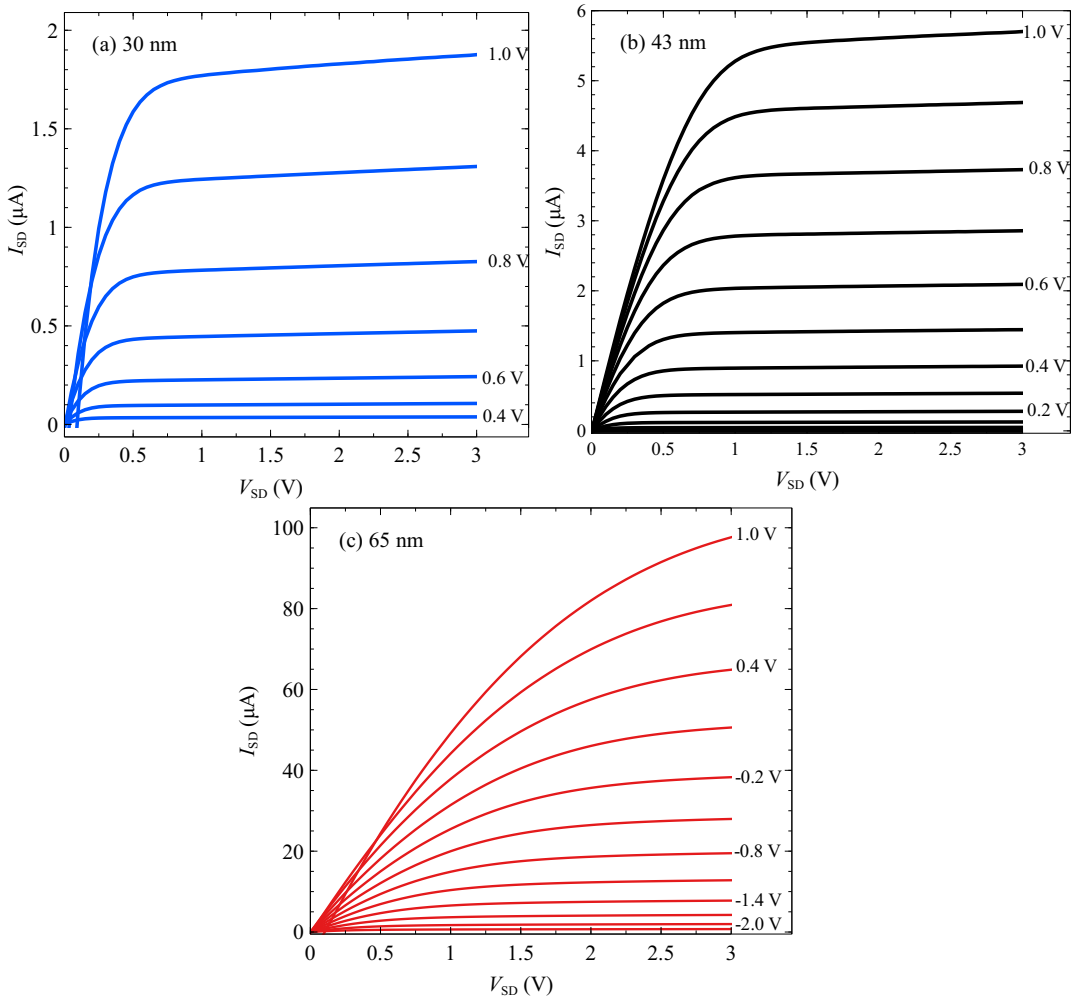


FIGURE 7.15: Output characteristic plots for a MESFETs devices defined by W/L = 100/5 μm fabricated on ZnO film active channel layers of thickness (a) 30nm (b) 43 nm and (c) 65 nm.

conducting layer. The transconductance plot in Fig. 7.14(b) follows a trend where increased transconductance is associated with thicker channel layer

Even though the net donor density is expected to be independent of the channel thickness for an intrinsic semiconductor, the number of free charge carriers available for conduction is proportional to the channel layer thickness. This accounts for the higher absolute gate voltage required to turn off the drain current for a relatively thick channel layer. Also, as the channel thickness increases, the gate controllability over the channel decreases, requiring a higher absolute gate voltage to completely cut-off current conduction. It is generally observed that transistor performance metrics such as off-state current, I_{on}/I_{off} ratio, channel mobility, transconductance, and threshold/turn-on voltage are all dependent on the thickness of the channel layers. For the MESFET structure defined with W/L = 100/5 μm that is fabricated on a 65 nm thick film, the extracted channel mobility μ_{ch} = 5.7 cm^2/V.s compared to values of 3.2 cm^2/V.s and 1.0 cm^2/V.s found for a transistors with channel thickness of 43nm and 30 nm respectively. This observation of channel mobility being dependent on the thickness of the conducting layer is consistent with other reports [76, 166] as the mobility of charge carriers through the channel is affected by interface traps and channel layer dislocations [84, 59]. For a relatively thick film as an active conducting channel, the carrier transport layer is farther away from the interface traps. Thus, the effect of interface traps on the carrier mobility is weaker in thicker channel layers.

TABLE 7.3: Schottky barrier and transistor properties for MESFET devices with gate W/L = 100/5 μm fabricated on ZnO channels of varying thicknesses.

Channel Thickness		30 nm	43nm	65 nm
Source-Gate Diode	RR	1.2×10^{8}	2.0×10^{7}	5.7×10^{8}
	I_0 (A)	3.3×10^{-17}	9.1×10^{-17}	1.1×10^{-17}
	η	1.52	1.82	1.1
	SBH (eV)	1.16	1.13	1.18
Trasistor Characteristics	I_{on}/I_{off}	7.5×10^{6}	1.7×10^{7}	2.0×10^{7}
	μ_{ch} (cm^2/V.s)	~1.0	~4.3	~5.7
	V_{ON} (V)	0	-0.48	-3.45
	V_{TH}[§] (V)	0.42	0.29	-2.20
	S (mV/dec)	85	118	125

[§] V_{TH} extrapolated from linear region of the transconductance plot.
RR : Rectification ratio

Comparison in the output plots in Fig. 7.15 shows that transistor output

drain current at a given gate voltage is maximum for the MESFET device with the thickest channel layer. All the devices exhibited typical transistor behaviour with clear pinch off and saturation of the drain current modulated by the gate voltage. As expected, the thickness of the channel layer affects the output drain current at a given gate voltage and source-drain current. At $V_G = 1$ V and with $V_{SD} = 3$ V, output drain current is measured to be 97 μA, 71 mA and 56 μA for MESFETs defined by gate W/L = 100/5 μm, fabricated on ZnO channel layers with thicknesses of 65 nm, 43 nm and 30 nm respectively.

A summary of performance characteristics for MESFETs fabricated on different layer thickness of ZnO films is shown in table 7.3. It can be generally concluded that the thickness of the channel layer has no substantial effect on the source-gate diode properties. This observation is expected since the source-gate diode should be dependent on the quality of the Schottky contact. However, when the Schottky contact serves as a gate as seen in the transistor performance metrics, the effect of channel layer thickness becomes apparent as depicted in differences in threshold/turn-on voltage and channel mobility among the samples.

7.5 Different Schottky gates

One of the important components of a MESFET is the gate for which its performance determines the overall characteristics of the transistor. A MESFET gate electrode with high Schottky barrier height and low leakage current is desirable to have good device performance. To compare the gate dependent performance characteristics, MESFETs were fabricated on samples of ZnO films using different oxidized metals as Schottky gate electrodes. Each of the devices was fabricated on a ZnO film deposited via the mist-CVD process with thickness of 65 nm. First, a thin film of ZnO that serves as a conducting channel was deposited on a 10 mm $\times$ 10 mm r-plane sapphire substrate, and diced into four pieces. This ensures that all samples used for the experiment have the same growth conditions and active layer thickness.

The fabricated MESFET devices employed a bi-layer of Ti/Au ($\sim$50 nm thick for each layer) as an ohmic contact electrode that is deposited using electron beam evaporation under vacuum (base pressure 10^{-6} mbar). For the Schottky gates, Ag, Pd, Ir, and Pt sputtering targets were used to reactively deposit $\sim$50 nm thick oxidized metal contacts for each fabricated device chip through RF sputtering technique. Argon gas was used as the

sputtering gas and is supplied into a vacuum deposition chamber at a flow rate of 10 sccm. Oxygen gas was used as a reactive gas to form oxidized metal oxides as Schottky gates instead of pure metals. The same deposition

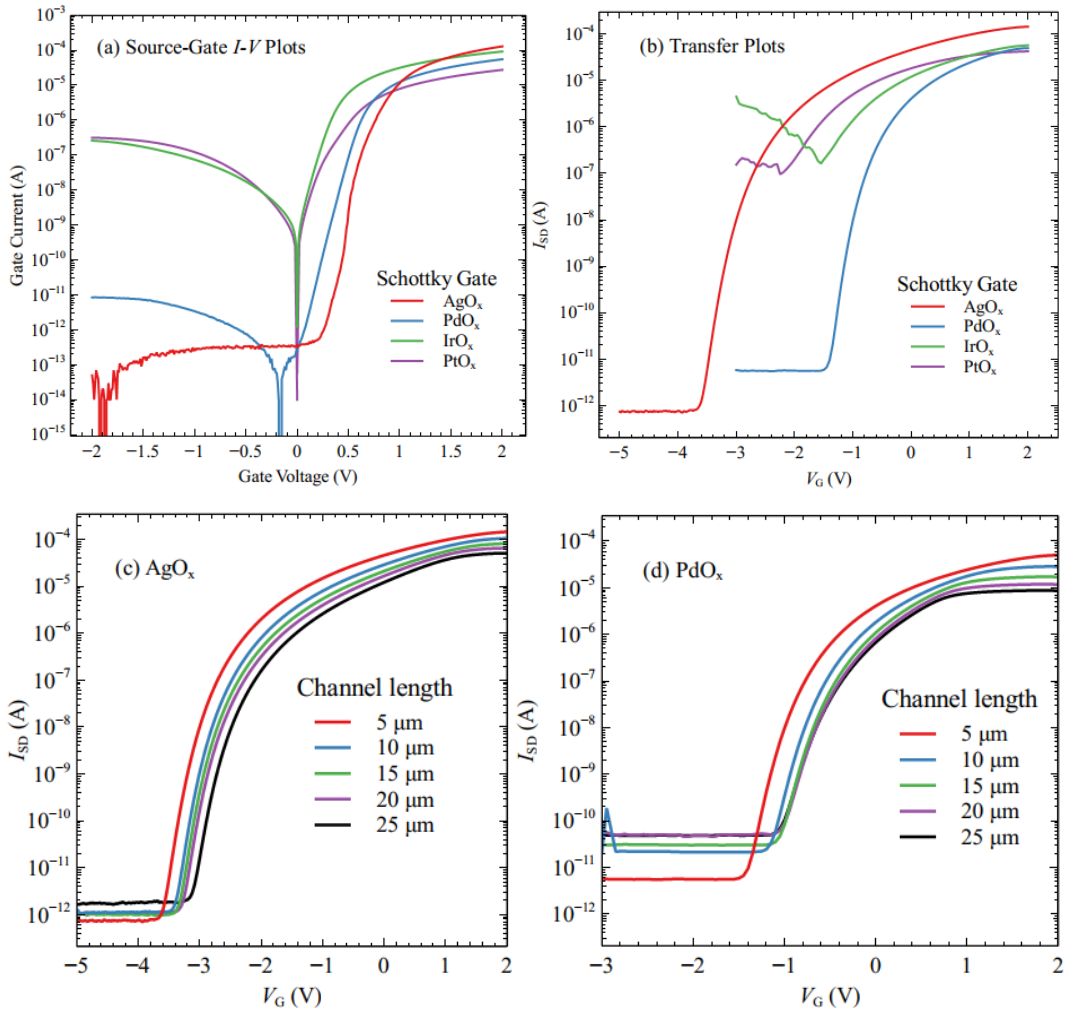


FIGURE 7.16: (a) Source-gate diode *I-V* plots and (b) Transfer characteristics of MESFETs defined by W/L = 100/5 μm fabricated with different gate materials. Transfer characteristics measured for MESFETs with varying gate length fabricated with Schottky gate made of (c) AgO_x (d) PdO_x.

conditions were maintained for the different Schottky gate materials investigated. Detailed fabrication steps including the deposition of metal contact electrodes have been outlined in section 6.3.7 of the previous chapter.

A comparison of performance parameters for MESFETs with different oxidized metals as Schottky gate is shown in Fig. 7.16. The source-gate diode characteristics shown in Fig. 7.16(a) indicates improved current rectification for the AgO_x and PdO_x gate contacts compared with IrO_x and PtO_x. Current rectification ratio RR is measured to be about 8 $\times 10^8$ and 6 $\times 10^6$ for the AgO_x

and PdO_x respectively. The SBH extracted for a PdO_x gate diode with $L \times W$ = 5 μm $\times$ 100 μm is 0.94 eV.

Both IrO_x and PtO_x gate contacts show inferior diode characteristics with current rectification ratio not exceeding two orders of magnitude. Since the gate contact serves to modulate the drain current in a field effect transistor device, a similar trend is shown in the transfer characteristics plots in Fig. 7.16(b). The maximum drain current I_{on}/I_{off} ratio was recorded for transistor device with the AgO_x gate. Despite the higher I_{on}/I_{off} ratio obtained for AgO_x Schottky gate, PdO_x showed lower turn-on and threshold voltages. This implies a lower operating voltage for the PdO_x gate device with less voltage required to turn on and turn off current conduction. Figs.7.16(c)-d show a gate length dependent transfer plots for MESFETs with AgO_x and PdO_x gate contacts. Output characteristics plots for MESFETs of varying gate lengths with AgO_x and PdO_x gates are shown in Fig. 7.17, confirming typical transistor characteristics. Deviation in the output curves at low V_{SD} and relatively high gate voltage seen for MESFETs with PtO_x Schottky gates is associated with gate leakage current across the barrier into the channel. MESFETs are inherently low-voltage devices for which gate leakage current signifies a violation of depletion region approximation leading to distortions in mathematical models for transistor characteristics curves.

All of the performance characteristics quantified with the diode, transfer and output measurements for PtO_x and IrO_x transistors showed inferior performance characteristics. These devices showed high leakage current and low Schottky barrier height without exhibiting the typical transistor characteristics. The results of a recent thesis [87] showed that the rectification ratio in oxidized noble metal Schottky contacts on bulk ZnO is dependent on the oxygen-to-argon gas ratio used during the sputtering of the metal contacts. Based on the work, increased field effect characteristics and higher barrier heights were achieved for oxidized metals (Ag, Ru, Pt, Ir, Pd) with higher oxygen-to-argon ratio used during the sputtering process (maximum Schottky rectification found for O_2 : Ar = 7:10 sccm). Despite using a O_2 : Ar ratio similar to the one used to gain maximum current rectification with least leakage current, IrO_x and PdO_x Schottky gates were still leaky.

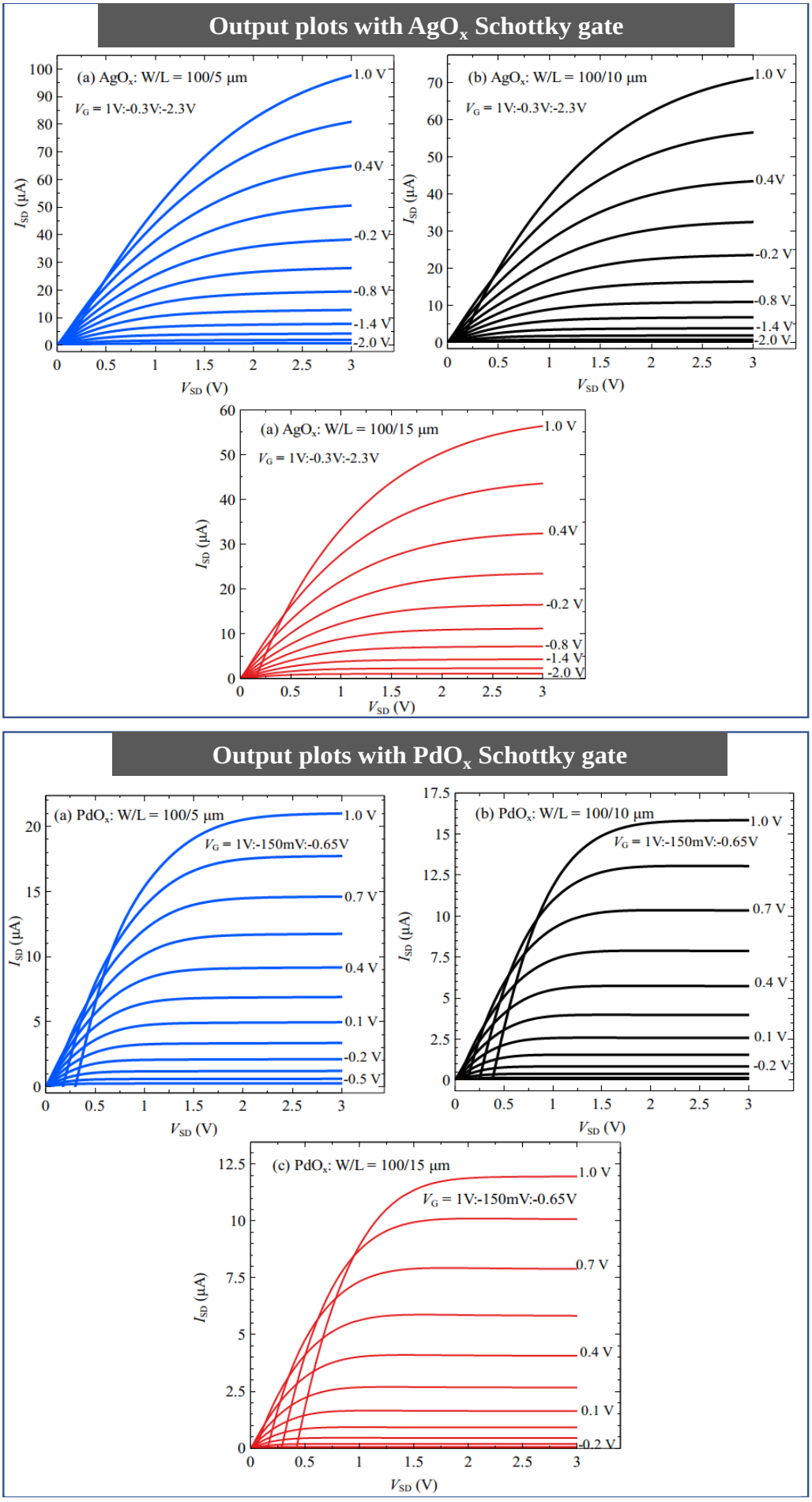


FIGURE 7.17: Output plots for selected MESFETs with AgO_x and PdO_x Schottky gates on a 65 nm thick ZnO channel layer.

Some of the probable reasons include the relatively higher number of film defects compared to bulk material or IrO_x and PtO_x forming metal contacts instead of oxidized metals during sputtering. Other reasons may be due to relatively higher thickness and increased charge carrier concentration of the 65 nm thick ZnO film used for the comparison. Further investigations to determine possible deposition conditions that could improve Schottky barrier properties for IrO_x and PtO_x were not carried out as part of my thesis. Focus was on AgOx which based on the experiment showed higher barrier height and current rectification. To date, AgO_x has been known to produce the highest barrier height in ZnO [87].

7.6 Device stability under bias stress

Stress measurement is important to determine the mechanisms that cause instability in device performance and to find out if the technology can be incorporated in integrated circuits. The stress test enables the operational stability of a device to be determined under prolonged electrical bias stress. The effect of a bias stress is attributed to the trapping of charge carriers into localized less mobile electronic states due to the gate bias voltage. These trap states may be localized within the semiconductor or at the semiconductor-metal interface. The longer the duration of the gate stress, the higher the number of trapped charge carriers. The trapped charge carriers can contribute to the charge balance in the transistor but not the drain current and manifests as shift in the threshold/turn-on voltage. Depending on the nature of the trapped states, trapped carriers can return to mobile states when the gate bias is removed or may require a physical elimination method such as thermal annealing.

A MESFET device structure with W/L = 100/10 μm was first subjected to a positive constant voltage stress (CVS) of 1.5 V at the gate while the source/drain terminal is grounded. Before the stress test, a no-stress condition was established by measuring the I_{SD} vs V_G transfer curve in the dark (V_{SD} = 3 V). Each step of the CVS experiment consists of increasing stress duration lasting from 1 seconds and then 10 seconds, 100 seconds and 1000 seconds. For each duration, a transfer characteristics curve is measured and a new stress duration is performed.

As illustrated in Fig. 7.18(a), a positive CVS introduced continuous negative shifts in the threshold/turn-on voltages for each increasing stress duration. There is also a degradation of performance resulting in an increase

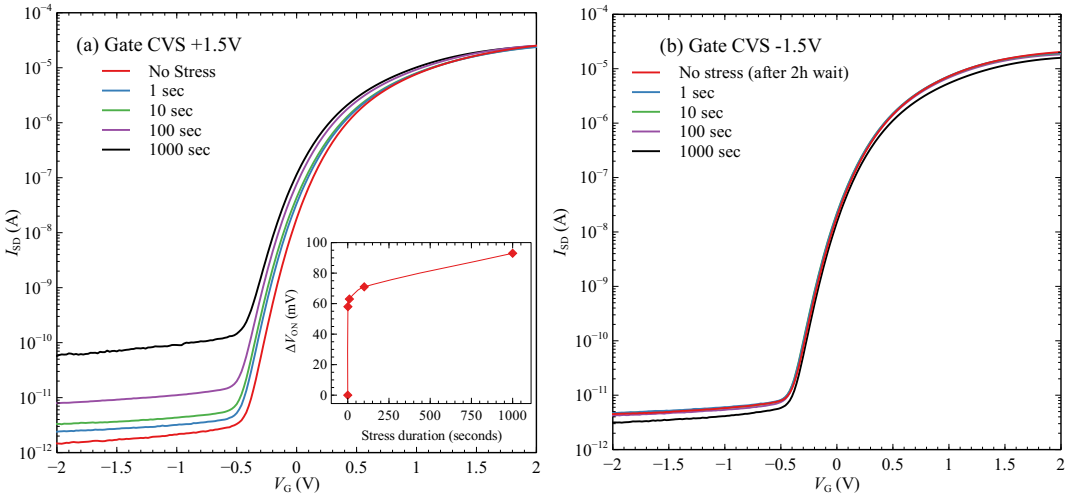


FIGURE 7.18: (a)Transfer characteristics plot for AgO_x MESFET with W/L = 100/10 μm under (a) gate CVS of 1.5 V for different durations in seconds (b) CVS of -1.5 V for different durations.

in the off-state current due to higher leakage current following the positive CVS. A positive voltage stress lasting for 1 second caused a shift ΔV_{ON} of 58 mV in V_{ON} which increased to 90 mV at 1000 seconds duration, as illustrated in the inset plot of Fig. 7.18(a). The shift in threshold voltage is attributed to the role of oxygen vacancies and holes. The degradation and recovery of device performance can be qualitatively explained based on charging and discharging of trap states at the gate/channel interface and within the channel region.

A positive voltage stress leads to attraction of electrons towards the interface trap states. As the stress duration increases, more of the trap states are filled. This leads to changes in the band bending and charge distribution arising from temporary electrons in the channel regions [36]. The increased number of electrons due to the positive CVS leads to reduction in the built-in potential, higher channel conductivity and thereby causing a negative shift in threshold voltage [23, 62]. Similarly, the higher off-state current is also explained by these changes where more induced oxygen vacancies accumulate in the interface leading to low channel resistivity.

Following the positive CVS and a wait period of 2 hours, the transfer characteristic was remeasured with no applied gate stress. The wait period with no stress allowed for changes induced due to the positive CVS on the gate to be reversed. Subsequently, the stability of device was assessed with a negative gate bias stress of V = -1.5 V under varying stress duration as shown in Fig. 7.18(b). The fact that the transfer characteristics recovered

to a near-original state after a period of relaxation, without any bias or thermal annealing suggests that instability in the device originates from interface states with short relaxation time even at room temperature [36]. The application of negative CVS on the gate after the relaxation period did not lead to any significant shift in the threshold/turn-on voltage. However, a slight decrease in the off-state current is observed with increased duration in the negative stress. The negative CVS reduces the number of trapped electrons on the interface with a resultant slight decrease in the on-current. Further application of negative stress on the gate tends to return the transistor to almost its original state. This varying characteristic behaviour under bipolar CVS on the gate is similar to other findings reported for ZnO based thin film transistors subjected to stress.

7.7 Elevated Temperature Measurement

Measurement of transistor characteristics was done at elevated temperature between 298 K - 403 K (25°C - 130°C). The experimental setup for elevated temperature measurement consisted of a parameter analyser (HP 4155A) and a probe station equipped with a Temptronic TP03000 temperature controller which allows for controlled heating of the sample stage of the prober. The *I-V* characteristic plots of the source-gate Schottky diode on a MESFET on a 43 nm thick ZnO film with W/L = 10/100 μm is shown in Fig. 7.19(a). The plot illustrates an increase in the forward bias gate current as the temperature is raised. Similarly, the reverse current increases as the temperature rises. This trend indicates the dominance of thermionic emission as the mechanism of current transport where the number of electrons with sufficient energy to cross the barrier increases with temperature.

The inset graph in Fig. 7.19(a) shows that the relationship between temperature change and the ideality factor is not uniform. It shows that an increase in temperature from 25°C to 65°C led to reduction in ideality factor with subsequent increase after 65°C. Similarly, the SBH moderately increased from 1.12 eV at room temperature up to 1.19 eV at 65°C. Further increase in temperature reduced the SBH to 0.9 eV at 130°C. The reduction of ideality factor (closer to unity) and an increase in SBH within the temperature range of 25°C - 65°C suggests that improvement in diode characteristics with temperature occurred within this temperature range. Due to increase in temperature of the electronic device, thermal energy improves electron injection

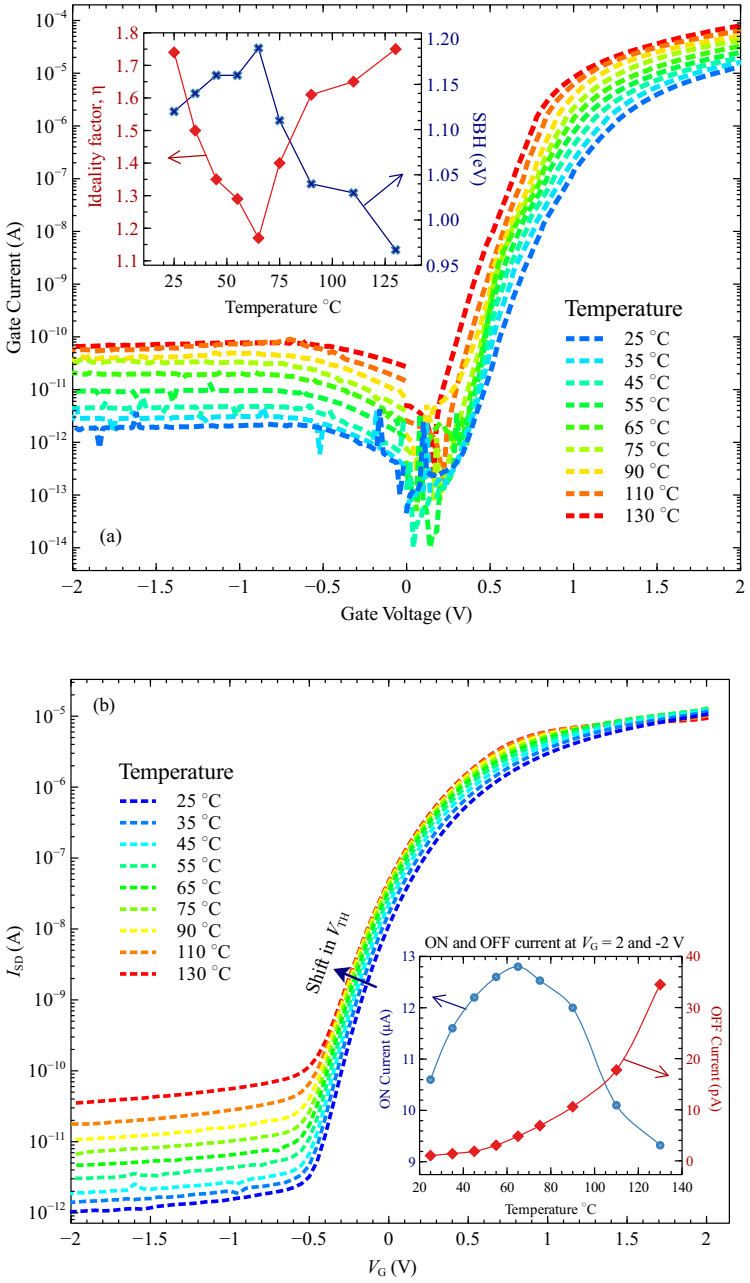


FIGURE 7.19: (a) *I-V* plots of the AgO_x Schottky gate diode of the a transistor device measured at elevated temperatures. Inset - Variation of barrier height and ideality factor with temperature (b) Temperature dependent transfer plots for a MESFET structure. Inset - Variation of off-current and I_{on}/I_{off} ratio with temperature.

efficiency through the Schottky barrier reducing the contact resistance. Additionally, the higher forward bias current results in a dramatic increase in the diode leakage current, approximately two orders of magnitude increase between temperature of 25°C - 130°C.

Temperature dependent transfer characteristics of the MESFET structure are shown in Fig. 7.19(b). The plot shows that the on-state drain current at $V_G = 2V$ did not show equivalent change similar to the dramatic increase in the off-current when the sample temperature increases. The off-state current increased from about 1 pA to 35 pA for a temperature change of 25 - 130°C whereas a small increase in the on-current was measured between the temperatures of 25°C - 65°C, and reduced with further temperature increase. Consistent with n-channel FETs, it is observed from the plot that a slight negative shift in the threshold voltage/turn-on voltage as temperature increases [134]. One of the popular explanations for this shift is associated with charge trapping mechanism which transfers mobile charges to immobile trap states at the gate interface [38, 116]. The higher the temperature, the higher the thermal energy required to activate charge carriers from trap states. Hence more absolute gate voltage is required to turn on or turn off the transistor at higher temperature [133].

The behaviour of the on-state drain current in the saturation region is explained by the relation: $I_{SD} \propto \mu(T)(V_G - V_{TH}(T))^2$ [134]. For moderate increase in sample temperature, an increase in $|V_G - V_{TH}|$ surpasses the effects of reduced charge carrier mobility leading to gradual increase in the drain current. However, with further temperature increase, mobility degradation results in the reduction of the drain current as shown on the inset plot of Fig. 7.19(b) where the on-state current in the saturation region is plotted against temperature. The on-state current increased up to a temperature of 65°C before it starts decreasing due to mobility degradation at higher temperature. A similar trend on ZnO Schottky characteristics with Ag as the gate was observed where the barrier height increased with a moderate increase in sample temperature [60]. The report shows a monotonic increase in barrier height was measured from 25 - 75°C, which further decreased beyond 75 °C. In addition, Klupfel *et al.* [116] reported a nearly constant transistor channel mobility up to 90°C which then dropped off beyond this temperature. The work of Ref. [51] also supports improvements in some ZnO MESFET performance metrics at moderately elevated temperature with channel mobility increase from room temperature to about 85°C, which then reduces with further increase in sample temperature.

It can be observed that the behaviour of the temperature dependent *I-V* measurement for the source-gate Schottky diode shows accompanying increase in both the forward bias and and reverse bias current with increase in temperature in contrast to the transfer characteristics plot. The reason for increased forward bias current for the diode measurement is that for diodes, electron injection efficiency arising from thermal effects contributes to the measured gate current while for the transfer properties of the transistor, current measured at the drain should ideally be dependent on the Schottky barrier properties of the gate electrode and not affected by the gate bias leakage current.

Another interesting observation from the plots shows that the performance characteristic of transistors fabricated on mist-CVD ZnO as channel layer is maintained at elevated temperature up to 130°C. This attribute supports the promising characteristics of ZnO for high temperature and high power electronic devices. Within the temperature range of 25 - 130°C, current leakage when the gate is under reverse bias increased by about 1.5 orders of magnitude whilst the gate retained its rectifying characteristics.

7.8 Sensitivity to UV light

The preceding discussions have presented performance characteristics for ZnO based MESFETs. However, instability in the performance of the devices is still an obstacle that needs attention. The effects of gate bias stress have already been explained in section 7.6. Apart from the stability of devices under bias stress, sensitivity to light is also of critical importance since many of the devices made from ZnO for use in digital display technologies will most likely get exposed to backlight or ambient light while in operation.

In the course of several *I-V* measurement done on our fabricated MESFET devices, no sensitivity in device performance was observed with exposure to visible light. A red LED light was used at the illumination source for the microscope for electrical characterization in the probe station. No detectable difference is observed for transistor performance characteristics measured whether the illumination red light is on or off during measurement. However, exposure of of MESFET structures to UV light during measurement induces a much more severe degradation in the device performance.

To test for UV response, an OmniCure® UV/visible mercury vapour lamp source with emission wavelength ranging from 320 - 500 nm was used to illuminate the transistor device while taking *I-V* characteristics measurements.

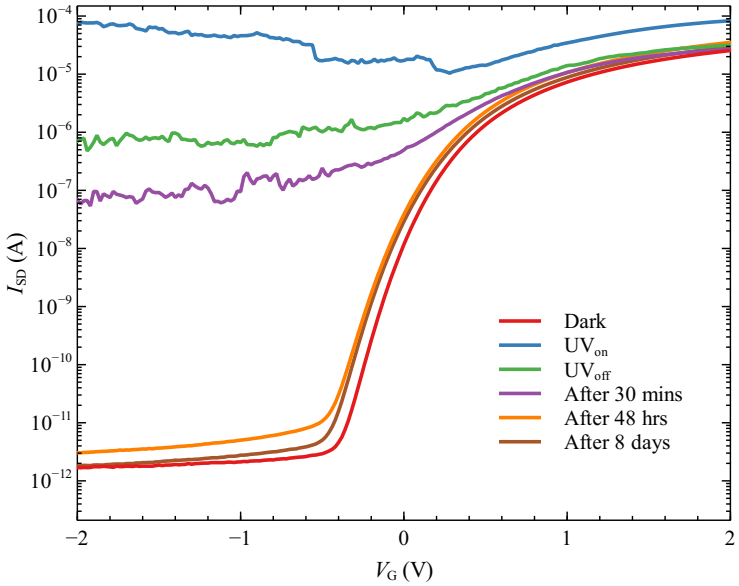


FIGURE 7.20: Transfer characteristic plots showing effects of UV illumination on on the performance of ZnO based MESFET device with gate $W/L = 100/10$ μm.

The intense UV illumination source (up to 30 W/cm^2) was kept on during an initial measurement. Immediately after the measurement, the UV light source was turned off and additional measurements were done. The photo-response to UV light illumination quantified through transfer characteristic plots of a MESFET device defined by gate $W/L = 100/10$ μm is shown in Fig. 7.20.

It can be seen that under UV illumination, a total breakdown of the Schottky barrier occurs with a giant increase in the off-state current by several orders of magnitude. This is associated with the effect of UV light on oxygen vacancies V_O, known to be the most abundant point defect in undoped ZnO. The report of Ping *et al.* [241] employed 8 μW/cm^2 monochromatic UV sources with wavelengths of 365 nm and 254 nm to illuminate ZnO thin film transistors for a duration of 2 minutes. Electrical measurements were carried out after the duration of UV exposure. In the report, an obvious degradation of transistor characteristics caused by photo-induced current in the off-state was observed ($\sim$ 10 - 10^2 increase of the dark current). Further, the exposure with a UV source of higher photon energy (254 nm wavelength; 4.88 eV) was observed to cause more severe transistor degradation compared with a 365 nm (3.40 eV) source. Similarly to the slight increase in the on-state current as shown in Fig. 7.20, UV illumination resulted in minimal effect on the on-state

current. The giant increase in the off-state current found in this work compared to the literature report may be associated with the marked difference in the power densities of the UV sources used for the experiments.

Based on theoretical studies, a high number of neutral oxygen vacancies V_O^0 can form as deep level states close to the top of the valence band (VB) maximum for ZnO [127]. Under illumination from UV light with photon energy greater than the bandgap energy, electron excitation from the valence band (VB) to the conduction band (CB) occurs in the ZnO channel. Additionally, the neutral oxygen vacancies V_O^0 are photo-excited, also donating electrons to the CB [127]. As a result, the off-current increases by several order of magnitude due to the UV light illumination. In contrast, the on-current increases by a small amount mainly because the on-current is dominated by the gate bias-induced charge carriers during UV irradiation of the transistor device [241].

As observed in the changes that occur after illumination, there is a state of residual conductivity. The off-current did not revert to its original dark current state even after the UV light source was removed for several days. This persistent conductivity effect may be attributed to the formation of ionized oxygen vacancies V_O^{2+} in the ZnO channel after UV illumination. During illumination, ground state oxygen vacancies V_O^0 are photo-excited to ionized oxygen vacancies V_O^{2+} with energy state below the CB minimum [127, 241]. Additionally, after the UV light is turned off, V_O^0 can also form the ionized V_O^{2+} by capturing the photo-excited holes in the valence band, also reducing direct recombinations. Further, after two holes are captured, the oxygen vacancies V_O undergo lattice distortion making the hole deeply trapped in the V_O^{2+} centres. For the V_O^{2+} to return to ground state V_O^0, an energy barrier has to be overcome by thermal activation [127, 241, 232]. This energy barrier slows down the recombination of electrons in the CB and holes trapped in the V_O^{2+}. It can be seen that the recovery of the dark off-state current is rather slow lasting several days post UV illumination.

7.9 Comparision with other reports

Many reports available on the literature on ZnO based transistor are mostly MISFETs, with only a few reports on MESFETs using ZnO film layer. The most likely reason is the difficulty in fabricating Schottky gate of high quality critical to successful operation of MESFET transistor devices. Table 7.4 lists

TABLE 7.4: Comparison of MESFET performance parameters fabricated on some ZnO based thin films as active channel.

Channel Film	d (nm)	Growth Method	n (cm^{-3})	μ_H $cm^2/(V.s)$	Gate Contact	SBH (eV)	μ_{ch} $cm^2/(V.s)$	I_{on}/I_{off}	S (mV/dec)	Ref
ZnO	30	mist-CVD	...	...	AgO_x	1.16	1.0	8×10^6	85	†
ZnO	43	mist CVD	3×10^{17}	8.0	AgO_x	1.13	4.3	1.7×10^7	118	†
ZnO	65	mist CVD	7.6×10^{17}	9.1	AgO_x	1.18	5.7	2.0×10^7	125	†
ZnO	20	PLD	5.5×10^{17}	9.3	AgO_x	1.0	11.3	2×10^8	...	[58]
ZTO	19	Sputtering	6.5×10^{17}	3.0	PtO_x	...	0.9	1.8×10^6	124	[224]
ZTO	22	mist-CVD	...	15.8	AgO_x	0.84	12	8×10^6	180	[40]
ZnO	20	PLD	4×10^{18}	20	PtO_x	...	9.5	1×10^5	130	[116]
GIZO	160	Sputtering	4.5×10^{16}	20.8	AgO_x	0.95	14.7	2.5×10^7	112	[141]
GIZO	145	mist-CVD	...	...	AgO_x	1.0	3.2	3.8×10^7	356	[39]
ZnO	55	FCVA	8×10^{17}	18	AgO_x	0.82	15	10^6	...	[52]

† Results obtained from the work of this thesis.

some reports available on ZnO related MESFETs and compares performance characteristics with results obtained in this thesis.

As can be seen on the table, performance characteristics found for MESFET devices fabricated on different thickness show comparable results with oxide films deposited by PLD and Sputtering technique. It can be seen from the comparison that the lowest value of sub-threshold slope was obtained for a MESFET device fabricated on a 30 nm thick film reported in this thesis. From review in the table, there is consistency in the choice of oxidized silver as the preferred gate material which has shown superior rectification characteristics among the noble metals. The SBH that is higher than 1 eV obtained for the fabricated devices reported in this work indicates that a good quality Schottky barrier can be achieved with mist-CVD deposited ZnO film.

As a concluding remark, it is of note that achieving a given transistor performance characteristics requires consideration of factors as well as trade-offs between the desired performance metric and its resultant demerits. For instance, a thicker semiconducting film as a channel potentially offers higher channel mobility, increased transconductance in addition to increased on-state current. However, the increased channel thickness is associated with higher absolute gate voltage needed to turn off current conduction leading to higher power requirement for device operation. A thick channel may also be more susceptible to increased leakage current. Most of the examples provided in this thesis to assess a given performance metric used the MESFET structure with the smallest gate length on the fabricated chip (i.e. 5μm). This is because the smallest gate length structure generally shows superior performance characteristics compared with longer gates. Shorter channels lead to larger carrier mobility across the transistor and faster switching of the transistor, desirable properties for high-frequency applications. Thus, transistor

miniaturization offered by smaller channels can lead to the increased packing density of transistors when used in an integrated circuit. Amidst the several advantages offered by continued miniaturization of transistors, there is still a limit to how small they are before performance is degraded by the so-called small channel effects. As of today, in what is generally referred to as technology nodes, transistors with gate lengths that are less than 10 nm are applicable in devices.

7.10 Summary

The Schottky barrier with high rectification ratio is formed on mist-CVD deposited ZnO films when contacted with oxidized silver (AgO_x) and oxidized palladium (PdO_x). The Schottky barrier height does not show any strong dependence on film thickness.

C-V analysis performed on a Schottky diode showed an expected decrease in capacitance as reverse bias voltage increasingly becomes negative. However, the accuracy of results obtained from Mott-Schottky analyses cannot be relied on since the semiconducting film has a relatively low intrinsic donor concentration and small thickness.

Transistor devices fabricated on mist-CVD grown ZnO films with AgO_x and PdO_x Schottky gates exhibit excellent transistor characteristics with output drain current modulated by the gate voltage.

The thickness of the ZnO channel affects almost all transistor performance metrics. Increased channel thickness is associated with higher transistor current output, increased transconductance and increased absolute gate voltage needed to turn on/turn off the device.

The turn-on voltages indicate that MESFET devices are depletion mode devices (i.e. normally on devices at a gate voltage of 0 V). The turn-on voltage also varies with the length and width of the gate.

Comparisons in the performance of transistors fabricated with different Schottky gate materials show that oxidized silver possesses superior gate characteristics based on rectification ratio and barrier height. PdO_x required lower turn-on voltage while IrO_x and PtO_x showed inferior diode characteristics with rectification below 2 orders of magnitude.

A positive constant voltage stress on the gate of AgO_x causes instability in the performance characteristics with an increase in the of-state current. Negative voltage stress has minimal effect on the transfer characteristics of the device.

Transistor characterization performed at elevated temperature indicate that transistor characteristics are maintained at 130°C, though with an increase in the off-state current.

Illumination of fabricated MESFET with a UV light source causes a breakdown of the Schottky barrier and leads to a giant increase in the off-state current. The original state of the transistor was not recovered after the removal of UV light source, with residual conductivity lasting for several days.

Chapter 8

Conclusions and Future Outlook

One of the key goals achieved in this research project was finding a novel method for the deposition of ZnO thin films on substrates employing non-volatile aqueous ammonia as a precursor solvent. This presents an interesting success for the mist-CVD growth of ZnO films where many of the reports in the literature have relied on volatile organic solvents such as acetone, methanol, and IPA either as a whole or mixed with deionized water. Volatile solvents present a significant safety risk and can constrain the upscaling of the mist-CVD growth technique as an industrial process. Additionally, utilizing mist-CVD deposited ZnO films as active channels in MESFETs presents another interesting aspect of the research in terms of the applicability of cheaply deposited films. Further, the project supports the very desirable merits of the mist-CVD growth technique as a cost-effective and safe method of depositing thin films of materials at atmospheric pressure, thus, avoiding some of the very expensive equipment used in PLD, MBE, and Sputtering techniques. A summary of the key findings of the research including some study limitations is discussed.

8.1 Film Deposition and Properties

8.1.1 Surface Morphology

Despite serving as a low-cost deposition method, ZnO films grown using the mist-CVD showed uniform film deposition across various substrates. The surface morphology of films is influenced by factors such as substrate, deposition temperature, film thickness, and precursor concentration. In general, analyses of AFM micrographs of ZnO film surfaces showed that film growths on the r-plane sapphire substrates have smoother surface topography compared with films on a c-plane sapphire substrate. Typical thickness dependent root-mean-square roughness ranges between R_{rms} = 2.2 nm - R_{rms}

= 4.3 nm for films deposited on r-plane sapphire substrates with thickness up to 260 nm. As film thickness increases, elongation of grains oriented in a given direction leading to surface anisotropy is noticed in films deposited on r-plane sapphire. Higher surface roughness parameters were obtained for growths on c-plane sapphire substrate with up to R_{rms} = 44 nm obtained on a 260 nm film sample.

8.1.2 Electrical properties

Most of the as-grown ZnO films deposited on r-plane sapphire with a substantial thickness (30 nm and above) were electrically conductive with a conducting path detectable with a resistance meter. Electrical characterization performed through Hall measurement showed that films are of n-type conductivity with charge carrier concentration, resistivity, and charge carrier mobility affected by factors such as film thickness, growth temperature, and annealing. Charge carrier concentration in the orders of 10^{19} cm^{-3} and mobility as high as 32 $\text{cm}^2/\text{V.s}$ were found for as-grown ZnO film sample with thickness of about 380 nm. Likewise, resistivity as low as 10^{-2} Ω-cm was achieved for the samples.

8.1.3 Crystalline properties

In terms of crystalline properties, XRD analyses showed that films exhibited the hexagonal wurtzite structure of ZnO with preferred growth orientation dependent on the substrate used for deposition. For growths on an r-plane sapphire substrate, the dominant diffraction peaks from ZnO indicate growth in nonpolar a-plane $(11\bar{2}0)$ crystallographic orientation. The dominant diffraction peak for films grown on c-plane sapphire is that of the (0002) crystal plane while for growth on an a-plane sapphire substrate, peaks from (0002) and $(10\bar{1}0)$ dominate the XRD pattern. Deposited ZnO films follow growth orientation that is consistent with the epitaxial relationship reported for ZnO films grown on different planes of the sapphire substrate. The XRD pattern for ZnO film grown on amorphous quartz substrate shows as a combination of polycrystalline phases with amorphous impurity in its texture. Growth temperature tends to affect crystallinity with the least broadening in the rocking curve scan obtained for film sample deposited at 550°C.

8.1.4 Optical properties

Deposited ZnO films were optically transparent in the visible region with a strong absorption edge corresponding to the bandgap of ZnO. Transparency in the visible region is more than 80% for all film samples irrespective of the film thickness. Using the Tauc method for bandgap extraction deposited films gave room temperature bandgap energy of between 3.27 - 3.32 eV that is dependent on the thickness of films. Temperature-dependent transmission studies on a ZnO film sample shows a temperature-dependent bandgap energy shifts that is blue-shifted as the temperature decreases, and fits well to theoretical models that describe shifts in bandgap energy with temperature. Fitting these models to our experimental data yielded fit results that are comparable to other reports in the literature.

Luminescence characteristics studied through PL spectroscopy show a strong UV emission peak in addition to a weak, broad emission peak in the visible region. Analyses of low-temperature PL spectra acquired at 4K show excitonic emission peaks associated with defects acting as donor and acceptor impurities. By comparing the energy positions of these peaks with available reports in the academic literature, it was concluded that donor bound excitonic peak centered at 3.362 eV originates from Al impurities. Also, the peak at 3.321 eV is attributed to substitutional nitrogen acting as an acceptor in the lattice. The most probable source of donor impurities is from the aluminum-made fine-channel reactor where Al can migrate to the ZnO film at the typical growth temperature. The origin of acceptor impurities is from aqueous ammonia which gives a nitrogen-rich environment during growth.

8.2 MESFET performance characteristics

ZnO films grown with the mist-CVD technique exhibited typical transistor characteristics when utilized as active conducting channels in MESFET devices. The performance metrics of devices are strongly influenced by the thickness of the channel layer. Higher channel mobility estimated to be 5.7 $cm^2/V.s$ was achieved for a transistor fabricated on a 65 nm film, with values of 4.3 $cm^2/V.s$ and 1.0 $cm^2/V.s$ found for a transistor on 43 and 30 nm thick channels respectively. The turn-on voltages for the transistor devices V_{ON} shows that fabricated devices were mainly depletion-mode MESFETs which are normally in on-state at zero gate bias voltage. Subthreshold swing as low as 85 mV/decade was obtained for a MESFET device fabricated on

a channel of 30 nm thickness. Another factor that affects transistor performance is the gate dimensions. In line with the theory of field-effect transistors, the current output on fabricated transistor devices is dependent on the width-to-length ratio (*W/L*) of the gate. The size and the geometry of the gate influence several metrics including transconductance, channel mobility, and threshold/turn-on voltage.

Comparison on MESFET performance for devices fabricated using AgO_x, PdO_x, IrO_x and PtO_x showed that transistor properties are dependent on the Schottky gate material. In terms of transistor I_{on}/I_{off} current ratio, AgO_x returned the maximum value. Despite the higher I_{on}/I_{off} ratio for obtained for the AgO_x based transistor, PdO_x gate contact however, resulted in reduced threshold voltage/turn-on voltage. MESFETs fabricated using IrO_x and PtO_x gate materials generally showed inferior performance both in terms of diode and transistor characteristics. The source-gate diode rectification ratio obtained for IrO_x and PtO_x is about 10^2.

Under elevated temperature, ZnO-based MESFET maintains expected field-effect transistor characteristics, though with an increase in leakage current and reduction in I_{on}/I_{off} ratio by about two orders of magnitude for a temperature increase of 25°C - 130°C. By subjecting the gate electrode of a MESFET device to positive constant voltage stress (CVS), an increase in off-state current was observed while a CVS of negative polarity has minimal effect on device functioning. Conversely, under illumination with intense UV light, transistor behavior and performance characteristics deteriorate with a breakdown of the Schottky barrier, lasting several days before full recovery to the original state.

8.3 Limitations of Research

There are some study limitations present during the research. Some of these limitations are discussed in addition to some possible ways of solving some issues encountered. For the growth of ZnO films using the mist-CVD technique, deposition temperature can be increased up to 500°C, with a noticeable deterioration in the aluminum-based reactor when growth temperature is increased further. Utilizing high melting point materials such as stainless steel and glass in the design of the reactor will eliminate this constraint and allow film growths at a higher temperature of 700°C and above. Further, photoluminescence spectroscopy indicated the presence of aluminum in deposited films. Aluminum is well reported to act as donor impurities

in ZnO. A non-aluminum based reactor system (e.g. stainless steel or glass) may eliminate this unintentional aluminum incorporation in deposited films and allow for the control of film electrical characteristics if needed.

The mist-CVD system potentially offers a wider scope in terms of applicability for doping, growth of multi-layer structures and complex oxide materials of various elemental compositions. However, our attempt to incorporate magnesium in ZnO thin films did not yield satisfactory results, most probably as a result of using a single ultrasonic atomizing unit. Improvement in doping and the ability to grow multi-layer structures can potentially be achieved by using multiple atomizing units that feed into a single deposition reactor. By using multiple atomizing units, the constituent solution of desired materials can be individually optimized with more understanding and predictability of chemical reactions that occur in each solution. For example, improved incorporation of magnesium in doped ZnO film will more likely occur when solutions of zinc acetate and magnesium acetate are individually mixed and atomized separately.

There are still some issues with reproducibility and consistency in the thickness of deposited films using the mist-CVD system. For instance, growth rate and film thickness are affected by several factors including precursor pH, temperature, concentration, as well as less prominent factors such as the position of the substrate in the reactor, direction of the mist flow, etc. Since any of these factors can affect the properties of films grown, standardized and reproducible means of experimental setup and measurement procedure needs to be maintained. This may be achieved by accurate and automated systems in the film deposition process.

Despite the excellent performance for MESFETs obtained on ZnO film as an active conducting channel while utilizing oxidized silver as the gate electrode, similar performance metrics were not obtained with other oxidized metals as Schottky gates investigated in this project. Further work involving other oxidized metal contacts for MESFETs fabricated on mist-CVD ZnO film may need to be undertaken. Additionally, while the MESFETs devices showed performance stability under illumination with red visible light, exposing the devices to UV light caused a significant deterioration in the performance with leakage current increasing by several orders of magnitude. The effect of UV light on device performance and the resulting persistent photoconductivity presents a significant potential limitation to utilizing ZnO based transistors for optoelectronic application since even an inadvertent exposure to UV light can cause performance instability in devices.

There are possible ways of solving the UV photosensitivity issues associated with fabricated MESFETs. One of the common methods is to use insulating passivation layers of materials such as silicon dioxide (SiO_2), hafnium oxide (HfO_2) or silicon nitride (Si_3N_4). The passivation layer therefore ideally protects the active semiconducting channel from factors in the surrounding environment that can cause device instability.

It will be an interesting future work for a more detailed investigation on UV photo-response and its associated persistent photo conductivity on mist-CVD deposited ZnO films. A recent thesis work from our research group investigated this effect on MBE grown ZnO film sample and found strong persistent photocurrent associated with UV illumination on a 170 nm thick sample [89]. Preliminary investigation conducted on our mist-CVD deposited ZnO films (without contacts) by passing current and measuring voltage through samples are not presented in this thesis. However, initial results show that a film sample with thickness of about 500 nm did not show any persistent photoconductivity effect when irradiated with UV lamp source. In contrast, ZnO film with thickness less than 100 nm had a dramatic increase in UV induced current due to illumination. Such a finding presents an interesting aspect which seems to suggest that UV photo-response is a surface sensitive effect and gets diminished as the thickness of film increases.

Bibliography

[1] NR Aghamalyan et al. "Influence of thermal annealing on optical and electrical properties of ZnO films prepared by electron beam evaporation". *Semiconductor science and technology* 18.6 (2003), p. 525.

[2] MW Allen, SM Durbin, and JB Metson. "Silver oxide Schottky contacts on n-type ZnO". *Applied Physics Letters* 91.5 (2007), p. 053512.

[3] MW Allen et al. "Bulk transport measurements in ZnO: The effect of surface electron layers". *Physical Review B* 81.7 (2010), p. 075211.

[4] MW Allen et al. "Oxidized noble metal Schottky contacts to n-type ZnO". *Applied Physics Letters* 94.10 (2009), p. 103508.

[5] Antonis N Andriotis and Madhu Menon. "Band gap engineering via doping: A predictive approach". *Journal of Applied Physics* 117.12 (2015), p. 125708.

[6] S Angappane, NR Selvi, and GU Kulkarni. "ZnO (101) films by pulsed reactive crossed-beam laser ablation". *Bulletin of Materials Science* 32.3 (2009), pp. 253–258.

[7] John R Arthur. "Molecular beam epitaxy". *Surface science* 500.1-3 (2002), pp. 189–217.

[8] M Asghar et al. "Investigation of temperature dependent barrier height of Au/ZnO/Si schottky diodes". *IOP Conference Series: Materials Science and Engineering*. Vol. 60. 1. IOP Publishing. 2014, p. 012041.

[9] ABM Almamun Ashrafi et al. "Nitrogen-doped p-type ZnO layers prepared with H2O vapor-assisted metalorganic molecular-beam epitaxy". *Japanese journal of applied physics* 41.11B (2002), p. L1281.

[10] V Assuncao et al. "Influence of the deposition pressure on the properties of transparent and conductive ZnO: Ga thin-film produced by rf sputtering at room temperature". *Thin Solid Films* 427.1-2 (2003), pp. 401–405.

[11] DM Bagnall et al. "MBE growth of high-quality ZnO" lms on epi-GaN Appl". *Phys. Lett.* 70 (1997), p. 2230.

[12] DM Bagnall et al. "Room temperature excitonic stimulated emission from zinc oxide epilayers grown by plasma-assisted MBE". *Journal of crystal growth* 184 (1998), pp. 605–609.

[13] *Band theory of solids*. 2019. URL: https://phys.libretexts.org/Bookshelves/University_Physics/Book%3A_University_Physics_(OpenStax)/Map%3A_University_Physics_III_-_Optics_and_Modern_Physics_(OpenStax)/9%3A_Condensed_Matter_Physics/9.5%3A_Band_Theory_of_Solids.

[14] P Barquinha et al. "The role of source and drain material in the performance of GIZO based thin-film transistors". *physica status solidi (a)* 205.8 (2008), pp. 1905–1909.

[15] G Bauer. "Elektrisches und optisches Verhalten von Halbleitern. XIII Messungen an Cd-, Tl-und Sn-Oxyden". *Annalen der Physik* 422.5 (1937), pp. 433–445.

[16] Davinder S. Bhachu. "The Synthesis and Characterization of metal oxide thin films". PhD Thesis. University College London, 2013.

[17] G Biasiol and L Sorba. "Molecular beam epitaxy: principles and applications". *Crystal growth of materials for energy production and energy-saving applications* (2001), pp. 66–83.

[18] Mario Birkholz. *Thin film analysis by X-ray scattering*. John Wiley & Sons, 2006.

[19] G Blattner et al. "Influence of magnetic fields up to 20 T on excitons and polaritons in CdS and ZnO". *Physical Review B* 25.12 (1982), p. 7413.

[20] C Boemare et al. "Photoluminescence studies in ZnO samples". *Physica B: Condensed Matter* 308 (2001), pp. 985–988.

[21] CI Bright. "Review of transparent conductive oxides (TCO)". *Mattox DM, Mattox VH (eds)* 50 (2007).

[22] Eric A Burgett et al. "Growth of ZnO for neutron detectors". *Chapter 12, Handbook of zinc oxide and related materials (by ZC Feng): Volume 2-Devices and Nano-Engineering, Published by CRC Press Taylor and Francis Group* (2012), pp. 435–483.

[23] Wensi Cai et al. "Transparent thin-film transistors based on sputtered electric double layer". *Materials* 10.4 (2017), p. 429.

[24] Peter Capper, Safa Kasap, and Arthur Willoughby. *Zinc oxide materials for electronic and optoelectronic device applications*. John Wiley & Sons, 2011.

[25] PF Carcia et al. "Transparent ZnO thin-film transistor fabricated by rf magnetron sputtering". *Applied Physics Letters* 82.7 (2003), pp. 1117–1119.

[26] CRA Catlow and AM Stoneham. "Ionicity in solids". *Journal of Physics C: Solid State Physics* 16.22 (1983), p. 4321.

[27] Austin Chambers. *Modern vacuum physics*. CRC Press, 2004.

[28] JJ Chen et al. "Deposition of high-quality zinc oxide thin films on diamond substrates for high-frequency surface acoustic wave filter applications". *Thin Solid Films* 485.1-2 (2005), pp. 257–261.

[29] Rongsheng Chen and Linfeng Lan. "Solution-processed metal-oxide thin-film transistors: a review of recent developments". *Nanotechnology* 30.31 (2019), p. 312001.

[30] Yefan Chen et al. "Layer-by-layer growth of ZnO epilayer on Al 2 O 3 (0001) by using a MgO buffer layer". *Applied Physics Letters* 76.5 (2000), pp. 559–561.

[31] MW Cho et al. "Issues in ZnO homoepitaxy". *Superlattices and Microstructures* 38.4-6 (2005), pp. 349–363.

[32] Hugh Churchill. "Growth and Exfoliation of Selenium and Tellurium for Quantum Chains of Atoms". *Microscopy and Microanalysis* 24.S1 (2018), pp. 1672–1673.

[33] BJ Coppa et al. "Structural, microstructural, and electrical properties of gold films and Schottky contacts on remote plasma-cleaned, n-type ZnO {0001} surfaces". *Journal of applied physics* 97.10 (2005), p. 103517.

[34] Jennifer B Coulter and Dunbar P Birnie III. "Assessing Tauc plot slope quantification: ZnO thin films as a model system". *physica status solidi (b)* 255.3 (2018), p. 1700393.

[35] SFJ Cox et al. "Experimental confirmation of the predicted shallow donor hydrogen state in zinc oxide". *Physical review letters* 86.12 (2001), p. 2601.

[36] RBM Cross et al. "A comparison of the performance and stability of ZnO-TFTs with silicon dioxide and nitride as gate insulators". *IEEE transactions on electron devices* 55.5 (2008), pp. 1109–1115.

[37] Bernard Dennis Cullity and Stuart R Stock. *Elements of X-ray Diffraction*. Vol. 3. Prentice hall New Jersey, 2001.

[38] AS Dahiya et al. "Stability evaluation of ZnO nanosheet based source-gated transistors". *Scientific reports* 9.1 (2019), pp. 1–11.

[39] Giang T Dang et al. "Stability of In-Ga-Zn-O metal-semiconductor field-effect-transistors under bias, illumination, and temperature stress". *Applied Physics Letters* 107.14 (2015), p. 143504.

[40] GT Dang et al. "Zinc tin oxide metal semiconductor field effect transistors and their improvement under negative bias (illumination) temperature stress". *Applied Physics Letters* 110.7 (2017), p. 073502.

[41] *Deposition Technology for beginnersl How MOCVD works*. 2019. URL: https://www.aixtron.com/innovation/technologien/How_MOCVD_works.pdf.

[42] Sarah Derbali et al. "Structural and optical properties of ZnO thin films grown by rapid atmospheric mist chemical vapor technique". *Optical and Quantum Electronics* 51.7 (2019), p. 210.

[43] Ping Ding et al. "Growth of p-type a-plane ZnO thin films on r-plane sapphire substrates by plasma-assisted molecular beam epitaxy". *Materials Letters* 71 (2012), pp. 18–20.

[44] R Dingle. "Luminescent transitions associated with divalent copper impurities and the green emission from semiconducting zinc oxide". *Physical Review Letters* 23.11 (1969), p. 579.

[45] María Teresa Doménech-Carbó and Laura Osete-Cortina. "Another beauty of analytical chemistry: chemical analysis of inorganic pigments of art and archaeological objects". *ChemTexts* 2.3 (2016), p. 14.

[46] Miguel Dominguez et al. "Metal-Semiconductor Interfaces in Thin-Film Transistors". *Different Types of Field-Effect Transistors: Theory and Applications* (2017), p. 103.

[47] Jian Du et al. "Highly transparent and conductive indium tin oxide thin films for solar cells grown by reactive thermal evaporation at low temperature". *Applied Physics A* 117.2 (2014), pp. 815–822.

[48] M Dutta, S Mridha, and D Basak. "Effect of sol concentration on the properties of ZnO thin films prepared by sol–gel technique". *Applied Surface Science* 254.9 (2008), pp. 2743–2747.

[49] *Electron Beam Evaporation*. 2019. URL: https://www.tungsten.com/tips/electron-beam-evaporation/.

[50] *Electrons and Holes in Semiconductors*. 2009. URL: https://people.eecs.berkeley.edu/~hu/Chenming-Hu_ch1.pdf.

[51] S Elzwawi et al. "Effect of Schottky gate type and channel defects on the stability of transparent ZnO MESFETs". *Semiconductor Science and Technology* 30.2 (2015), p. 024008.

[52] S Elzwawi et al. "Stable n-channel metal-semiconductor field effect transistors on ZnO films deposited using a filtered cathodic vacuum arc". *Applied Physics Letters* 101.24 (2012), p. 243508.

[53] Lorenzo Fanni et al. "Increasing polycrystalline zinc oxide grain size by control of film preferential orientation". *Crystal Growth & Design* 15.12 (2015), pp. 5886–5891.

[54] E Fortunato et al. "Recent advances in ZnO transparent thin film transistors". *Thin solid films* 487.1-2 (2005), pp. 205–211.

[55] OA Fouad et al. "Zinc oxide thin films prepared by thermal evaporation deposition and its photocatalytic activity". *Applied Catalysis B: Environmental* 62.1-2 (2006), pp. 144–149.

[56] Sami Franssila. *Introduction to microfabrication*. John Wiley & Sons, 2010.

[57] H Frenzel et al. "ZnO-based metal-semiconductor field-effect transistors with Ag-, Pt-, Pd-, and Au-Schottky gates". *Thin Solid Films* 518.4 (2009), pp. 1119–1123.

[58] H Frenzel et al. "ZnO metal-semiconductor field-effect transistors with Ag-Schottky gates". *Applied Physics Letters* 92.19 (2008), p. 192108.

[59] Heiko Frenzel. "ZnO-based metal-semiconductor field effect transistors". PhD Dissertation. Universität Leipzig.

[60] Heiko Frenzel et al. "Recent Progress on ZnO-Based Metal-Semiconductor Field-Effect Transistors and Their Application in Transparent Integrated Circuits". *Advanced Materials* 22.47 (2010), pp. 5332–5349.

[61] Zhuxi Fu et al. "The effect of Zn buffer layer on growth and luminescence of ZnO films deposited on Si substrates". *Journal of crystal growth* 193.3 (1998), pp. 316–321.

[62] Tze-Ching Fung et al. "Electrical instability of RF sputter amorphous In-Ga-Zn-O thin-film transistors". *Journal of Display Technology* 5.12 (2009), pp. 452–461.

[63] Abdel-Sattar Gadallah and MM El-Nahass. "Structural, optical constants and photoluminescence of ZnO thin films grown by sol-gel spin coating". *Advances in Condensed Matter Physics* 2013 (2013).

[64] D Gal et al. "Electrochemical deposition of zinc oxide films from non-aqueous solution: a new buffer/window process for thin film solar cells". *Thin Solid Films* 361 (2000), pp. 79–83.

[65] T Ganesh et al. "Effect of Thickness on Micro-Structural and Optical Properties of Al-Doped ZnO Films Prepared by Sol-Gel Spin Coating". *Nano Hybrids and Composites*. Vol. 17. Trans Tech Publ. 2017, pp. 171–178.

[66] Jingyun Gao et al. "Compensation mechanism in N-doped ZnO nanowires". *Nanotechnology* 21.24 (2010), p. 245703.

[67] R Ghosh, D Basak, and Shinobu Fujihara. "Effect of substrate-induced strain on the structural, electrical, and optical properties of polycrystalline ZnO thin films". *Journal of Applied Physics* 96.5 (2004), pp. 2689–2692.

[68] Bernard Gil. "Oscillator strengths of A, B, and C excitons in ZnO films". *Physical Review B* 64.20 (2001), p. 201310.

[69] CR Gorla et al. "Structural, optical, and surface acoustic wave properties of epitaxial ZnO films grown on (0112) sapphire by metalorganic chemical vapor deposition". *Journal of Applied Physics* 85.5 (1999), pp. 2595–2602.

[70] Cecilie S Granerød et al. "The temperature-dependency of the optical band gap of ZnO measured by electron energy-loss spectroscopy in a scanning transmission electron microscope". *Journal of Applied Physics* 123.14 (2018), p. 145111.

[71] M Grundmann. *The physics of seminconductors: an introduction including nanoparticles and applications*. 2010.

[72] Marius Grundmann et al. "Transparent semiconducting oxides: Materials and devices". *Physica status solidi (a)* 207.6 (2010), pp. 1437–1449.

[73] *Gwyddion user guide*. 2019. URL: http://gwyddion.net/documentation/user-guide-en/index.html.

[74] K Haga, PS Wijesena, and H Watanabe. "Group III impurity doped ZnO films prepared by atmospheric pressure chemical–vapor deposition using zinc acetylacetonate and oxygen". *Applied surface science* 169 (2001), pp. 504–507.

[75] DW Hamby et al. "Temperature dependent exciton photoluminescence of bulk ZnO". *Journal of applied physics* 93.6 (2003), pp. 3214–3217.

[76] Dedong Han et al. "Effects of channel layer thickness on characteristics of flexible nickel-doped zinc oxide thin-film transistors". *IEEE Transactions on Electron Devices* 64.5 (2017), pp. 1997–2000.

[77] SK Han et al. "Structural and optical properties of non-polar A-plane ZnO films grown on R-plane sapphire substrates by plasma-assisted molecular-beam epitaxy". *Journal of Crystal Growth* 309.2 (2007), pp. 121–127.

[78] Jr-Hau He et al. "Development of Ohmic nanocontacts via surface modification for nanowire-based electronic and optoelectronic devices: ZnO nanowires as an example". *Nanoscale* 4.11 (2012), pp. 3399–3404.

[79] MS Hegde. "Epitaxial oxide thin films by pulsed laser deposition: retrospect and prospect". *Journal of Chemical Sciences* 113.5-6 (2001), pp. 445–458.

[80] R Heinhold et al. "Mobility of indium on the ZnO (0001) surface". *Applied Physics Letters* 106.5 (2015), p. 051606.

[81] Paul Heremans et al. "Mechanical and Electronic Properties of Thin-Film Transistors on Plastic, and Their Integration in Flexible Electronic Applications". *Advanced Materials* 28.22 (2016), pp. 4266–4282.

[82] Fred S Hickernell. "Zinc-oxide thin-film surface-wave transducers". *Proceedings of the IEEE* 64.5 (1976), pp. 631–635.

[83] IG Hill. "Numerical simulations of contact resistance in organic thin-film transistors". *Applied Physics Letters* 87.16 (2005), p. 163505.

[84] RL Hoffman, Benjamin J Norris, and JF Wager. "ZnO-based transparent thin-film transistors". *Applied Physics Letters* 82.5 (2003), pp. 733–735.

[85] JJ Hopfield. "JJ Hopfield, J. Phys. Chem. Solids 15, 97 (1960)." *J. Phys. Chem. Solids* 15 (1960), p. 97.

[86] Kai Huang et al. "Preparation and characterization of Mg-doped ZnO thin films by sol–gel method". *Applied Surface Science* 258.8 (2012), pp. 3710–3713.

[87] Alana Marie Hyland. "Noble Metal-Oxide Schottky Contacts on Zinc Oxide". PhD Thesis. University of Canterbury.

[88] AM Hyland et al. "Giant improvement in the rectifying performance of oxidized Schottky contacts to ZnO". *Journal of Applied Physics* 121.2 (2017), p. 024501.

[89] Adam Russell Hyndman. "Characterization of Thin Film ZnO Grown by Plasma Assisted Molecular Beam Epitaxy". PhD Thesis. University of Canterbury, 2017.

[90] Andrea Illiberi et al. "Recent Advances in Atmospheric Vapor-Phase Deposition of Transparent and Conductive Zinc Oxide". *Chemical Vapor Deposition* 20.7-8-9 (2014), pp. 234–242.

[91] K Ip et al. "Contacts to zno". *Journal of crystal growth* 287.1 (2006), pp. 149–156.

[92] MS Islam et al. "Zinc oxide thin film fabricated by thermal evaporation method for water splitting application". *2015 International Conference on Electrical & Electronic Engineering (ICEEE)*. IEEE. 2015, pp. 253–256.

[93] I Jacques. *Pankove, Optical Processes in Semiconductors*. 1971.

[94] Chennupati Jagadish and Stephen J Pearton. *Zinc oxide bulk, thin films and nanostructures: processing, properties, and applications*. Elsevier, 2011.

[95] Anderson Janotti and Chris G Van de Walle. "Native point defects in ZnO". *Physical Review B* 76.16 (2007), p. 165202.

[96] Hye-ji Jeon et al. "Enhanced mobility of Li-doped ZnO thin film transistors fabricated by mist chemical vapor deposition". *Applied Surface Science* 301 (2014), pp. 358–362.

[97] Hye-Ji Jeon et al. "Growth behaviors and film properties of zinc oxide grown by atmospheric mist chemical vapor deposition". *Journal of Alloys and Compounds* 614 (2014), pp. 244–248.

[98] Min-Chang Jeong et al. "Comparative study on the growth characteristics of ZnO nanowires and thin films by metalorganic chemical vapor deposition (MOCVD)". *Journal of Crystal Growth* 268.1 (2004), pp. 149–154.

[99] Taehwan Jun et al. "High-performance low-temperature solution-processable ZnO thin film transistors by microwave-assisted annealing". *Journal of Materials Chemistry* 21.4 (2011), pp. 1102–1108.

[100] Martin Kaltenbrunner et al. "Ultrathin and lightweight organic solar cells with high flexibility". *Nature communications* 3 (2012), p. 770.

[101] Y Kashiwaba et al. "Hetero-epitaxial growth of ZnO thin films by atmospheric pressure CVD method". *Journal of Crystal Growth* 221.1-4 (2000), pp. 431–434.

[102] Vipin K Kaushik et al. "Growth and characterization of ZnO and MgxZn1-xO thin films by aerosol assisted chemical vapor deposition technique". *Thin Solid Films* 520.9 (2012), pp. 3505–3509.

[103] Toshiyuki Kawaharamura. "Physics on development of open-air atmospheric pressure thin film fabrication technique using mist droplets: Control of precursor flow". *Japanese Journal of Applied Physics* 53.5S1 (2014), 05FF08.

[104] Toshiyuki Kawaharamura and Shizuo Fujita. "An approach for single crystalline zinc oxide thin films with fine channel mist chemical vapor deposition method". *physica status solidi c* 5.9 (2008), pp. 3138–3140.

[105] Toshiyuki Kawaharamura, Hiroyuki Nishinaka, and Shizuo Fujita. "Growth of crystalline zinc oxide thin films by fine-channel-mist chemical vapor deposition". *Japanese Journal of Applied Physics* 47.6R (2008), p. 4669.

[106] LAWRENCE L Kazmerski. "Electrical properties of polycrystalline semiconductor thin films". *Polycrystalline and amorphous thin films and devices*. Academic Press, 1980, pp. 59–133.

[107] Ziaul Raza Khan et al. "Optical and structural properties of ZnO thin films fabricated by sol-gel method". *Materials Sciences and applications* 2.05 (2011), p. 340.

[108] H Kim et al. "Electrical, optical, and structural properties of indium–tin–oxide thin films for organic light-emitting devices". *Journal of Applied Physics* 86.11 (1999), pp. 6451–6461.

[109] Han-Ki Kim et al. "Inductively-coupled-plasma reactive ion etching of ZnO using BCl3-based plasmas and effect of the plasma treatment on Ti/Au ohmic contacts to ZnO". *Thin Solid Films* 447 (2004), pp. 90–94.

[110] Hogyoung Kim. "Capacitance-voltage (CV) characteristics of Cu/n-type InP Schottky diodes". *Transactions on Electrical and Electronic Materials* 17.5 (2016), pp. 293–296.

[111] Jung-Hyun Kim et al. "Growth and structural properties of ZnO films on (10- 10) m-plane sapphire substrates by plasma-assisted molecular beam epitaxy". *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena* 27.3 (2009), pp. 1625–1630.

[112] HH King, J Lowe Hall, and Glen C Ware. "A study of the density, surface tension and adsorption in the water-ammonia system at 20". *Journal of the American Chemical Society* 52.12 (1930), pp. 5128–5135.

[113] Thomas Kirchartz et al. "Sensitivity of the Mott–Schottky analysis in organic solar cells". *The Journal of Physical Chemistry C* 116.14 (2012), pp. 7672–7680.

[114] C Klingshirn. "The luminescence of ZnO under high one-and two-quantum excitation". *physica status solidi (b)* 71.2 (1975), pp. 547–556.

[115] Claus F Klingshirn. *Semiconductor optics*. Springer Science & Business Media, 2012.

[116] Fabian Johannes Klüpfel et al. "Comparison of ZnO-based JFET, MESFET, and MISFET". *IEEE transactions on electron devices* 60.6 (2013), pp. 1828–1833.

[117] O Kluth et al. "Texture etched ZnO: Al coated glass substrates for silicon based thin film solar cells". *Thin solid films* 351.1-2 (1999), pp. 247–253.

[118] Hang Ju Ko et al. "MBE growth of high-quality ZnO films on epi-GaN". *Journal of Crystal Growth* 209.4 (2000), pp. 816–821.

[119] AF Kohan et al. "First-principles study of native point defects in ZnO". *Physical Review B* 61.22 (2000), p. 15019.

[120] Dominik Kohl. "The influence of energetic bombardment on the structure formation of sputtered zinc oxide films". PhD Thesis. RWTH Aachen University, 2011.

[121] D Korucu and S Duman. "Frequency and temperature dependent interface states and series resistance in Au/SiO2/p-Si (MIS) Diode". *Science of advanced materials* 7.7 (2015), pp. 1291–1297.

[122] Ching-Shun Ku et al. "Epitaxial growth of m-plane ZnO thin films on (1010) sapphire substrate by atomic layer deposition with interrupted flow". *Crystal Growth & Design* 10.4 (2010), pp. 1460–1463.

[123] LM Kukreja and P Misra. "Photoluminescence Processes in ZnO Thin Films and Quantum Structures". *ZnO Nanocrystals and Allied Materials*. Springer, 2014, pp. 49–89.

[124] E Senthil Kumar, Shubra Singh, and MS Ramachandra Rao. "Zinc Oxide: The Versatile Material with an Assortment of Physical Properties". *ZnO Nanocrystals and Allied Materials*. Springer, 2014, pp. 1–38.

[125] Manda Prashanth Kumar, Karunakaran Logesh, and Soumya Dutta. "Limitations of Mott-Schottky Analysis for Organic Metal-Insulator-Semiconductor Capacitors". *International Workshop on the Physics of Semiconductor and Devices*. Springer. 2017, pp. 69–74.

[126] A Lajn et al. "Properties of reactively sputtered Ag, Au, Pd, and Pt Schottky contacts on n-type ZnO". *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena* 27.3 (2009), pp. 1769–1773.

[127] Stephan Lany and Alex Zunger. "Dopability, intrinsic conductivity, and nonstoichiometry of transparent conducting oxides". *Physical Review Letters* 98.4 (2007), p. 045501.

[128] Chongmu Lee, Yeonkyu Park, and Kyungha Kim. "Effects of the Crystallographic Orientation of the Al2O3 Substrate on the Structural and the Optical Properties of ZnO Thin Films". *Journal of Korean Physical Society* 48.6 (2006), p. 1570.

[129] Deuk-Hee Lee et al. "Evaluation of acceptor binding energy of nitrogen-doped zinc oxide thin films grown by dielectric barrier discharge in pulsed laser deposition". *Transactions on Electrical and Electronic Materials* 12.5 (2011), pp. 200–203.

[130] Min-Hung Lee, B-F Hsieh, and ST Chang. "Electrical properties correlated with redistributed deep states in a-Si: H thin-film transistors on flexible substrates undergoing mechanical bending". *Thin Solid Films* 528 (2013), pp. 82–85.

[131] Youngjin Lee, Hagbong Kim, and Yongrae Roh. "Deposition of ZnO thin films by the ultrasonic spray pyrolysis technique". *Japanese Journal of Applied Physics* 40.4R (2001), p. 2423.

[132] Johann Gottlob Leidenfrost. "On the fixation of water in diverse fire". *International Journal of Heat and Mass Transfer* 9.11 (1966), pp. 1153–1166.

[133] Joseph A Letizia et al. "Variable Temperature Mobility Analysis of n-Channel, p-Channel, and Ambipolar Organic Field-Effect Transistors". *Advanced Functional Materials* 20.1 (2010), pp. 50–58.

[134] Zhao Lian-Feng et al. "GaSb p-channel metal-oxide-semiconductor field-effect transistor and its temperature dependent characteristics". *Chinese Physics B* 24.1 (2015), p. 018501.

[135] Huiyong Liu et al. "Transparent conducting oxides for electrode applications in light emitting and absorbing devices". *Superlattices and Microstructures* 48.5 (2010), pp. 458–484.

[136] Stergios Logothetidis. *Handbook of flexible organic electronics: Materials, manufacturing and applications*. Elsevier, 2014.

[137] David C Look, Joseph W Hemsky, and JR Sizelove. "Residual native shallow donor in ZnO". *Physical review letters* 82.12 (1999), p. 2552.

[138] David C Look and Richard J Molnar. "Degenerate layer at GaN/sapphire interface: Influence on Hall-effect measurements". *Applied Physics Letters* 70.25 (1997), pp. 3377–3379.

[139] David C Look et al. "Characterization of homoepitaxial p-type ZnO grown by molecular beam epitaxy". *Applied physics letters* 81.10 (2002), pp. 1830–1832.

[140] WT Lord. "Kelvin. Hydrokinetic solutions and observations". *Phil. Magazine* 42 (1871), pp. 362–377.

[141] M Lorenz et al. "Low-temperature processed Schottky-gated field-effect transistors based on amorphous gallium-indium-zinc-oxide thin films". *Applied Physics Letters* 97.24 (2010), p. 243506.

[142] Alex M Ma et al. "Zinc oxide thin film transistors with Schottky source barriers". *Solid-State Electronics* 76 (2012), pp. 104–108.

[143] JG Ma et al. "Method of control of nitrogen content in ZnO films: Structural and photoluminescence properties". *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena* 22.1 (2004), pp. 94–98.

[144] Jin Ma et al. "Preparation and properties of transparent conducting zinc oxide and aluminium-doped zinc oxide films prepared by evaporating method". *Solar Energy Materials and Solar Cells* 60.4 (2000), pp. 341–348.

[145] Marc J Madou. *Fundamentals of microfabrication: the science of miniaturization*. CRC press, 2002.

[146] Hiroaki Matsui et al. "Characteristics of polarity-controlled ZnO films fabricated using the homoepitaxy technique". *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena* 22.5 (2004), pp. 2454–2461.

[147] Rajesh Menon et al. "Maskless lithography". *Materials Today* 8.2 (2005), pp. 26–33.

[148] *Methanol Safe Handling Manual*. URL: http://www.methanol.org/wp-content/uploads/2017/03/Safe-Handling-Manual.pdf.

[149] BK Meyer et al. "Bound exciton and donor–acceptor pair recombinations in ZnO". *physica status solidi (b)* 241.2 (2004), pp. 231–260.

[150] Stephen T Meyers et al. "Aqueous inorganic inks for low-temperature fabrication of ZnO TFTs". *Journal of the American Chemical Society* 130.51 (2008), pp. 17603–17609.

[151] Paul Miller. "ZINC OXIDE: A SPECTROSCOPIC INVESTIGATION OF BULK CRYSTALS AND THIN FILMS A". PhD thesis. University of Canterbury, 2008.

[152] Tadatsugu Minami et al. "Group III impurity doped zinc oxide thin films prepared by RF magnetron sputtering". *Japanese journal of applied physics* 24.10A (1985), p. L781.

[153] Kazunori Minegishi et al. "Growth of p-type zinc oxide films by chemical vapor deposition". *Japanese Journal of Applied Physics* 36.11A (1997), p. L1453.

[154] Umesh Mishra and Jasprit Singh. *Semiconductor device physics and design*. Springer Science & Business Media, 2007.

[155] Poornima Mittal et al. "Channel length variation effect on performance parameters of organic field effect transistors". *Microelectronics Journal* 43.12 (2012), pp. 985–994.

[156] Constantin E Morosanu. *Thin films by chemical vapour deposition*. Vol. 7. Elsevier, 2016.

[157] VD Mote, Y Purushotham, and BN Dole. "Williamson-Hall analysis in estimation of lattice strain in nanometer-sized ZnO particles". *Journal of Theoretical and Applied Physics* 6.1 (2012), p. 6.

[158] TE Murphy et al. "Properties of electrical contacts on bulk and epitaxial n-type ZnO". *Journal of electronic materials* 34.4 (2005), pp. 389–394.

[159] JF Muth et al. "Excitonic structure and absorption coefficient measurements of ZnO single crystal epitaxial films deposited by pulsed laser deposition". *Journal of Applied Physics* 85.11 (1999), pp. 7884–7887.

[160] Keigo Nagao and Erina Kagami. "X-ray thin film measurement techniques VII. Pole figure measurement". *The Rigaku Journal* 27.2 (2011), pp. 6–14.

[161] Giwoong Nam et al. "Growth and optical properties of sol-gel ZnO thin films grown on R-plane sapphire substrates". *Journal of the Korean Physical Society* 62.8 (2013), pp. 1154–1159.

[162] Y Natsume and H Sakata. "Zinc oxide films prepared by sol-gel spin-coating". *Thin solid films* 372.1 (2000), pp. 30–36.

[163] Hiroyuki Nishinaka et al. "Epitaxial ZnO thin films on a-plane sapphire substrates grown by ultrasonic spray-assisted mist chemical vapor deposition". *Japanese Journal of Applied Physics* 48.12R (2009), p. 121103.

[164] M Novotnỳ et al. "Structural characterization of ZnO thin films grown on various substrates by pulsed laser deposition". *Journal of Physics D: Applied Physics* 45.22 (2012), p. 225101.

[165] Fumiyasu Oba et al. "Energetics of native defects in ZnO". *Journal of Applied Physics* 90.2 (2001), pp. 824–828.

[166] Byeong-Yun Oh et al. "Effects of the channel thickness on the structural and electrical characteristics of room-temperature fabricated ZnO thin-film transistors". *Semiconductor science and technology* 22.6 (2007), p. 608.

[167] Takeshi Ohgaki et al. "Growth condition dependence of morphology and electric properties of ZnO films on sapphire substrates prepared by molecular beam epitaxy". *Journal of Applied Physics* 93.4 (2003), pp. 1961–1965.

[168] Eriko Ohshima et al. "Growth of the 2-in-size bulk ZnO single crystals by the hydrothermal method". *Journal of Crystal Growth* 260.1 (2004), pp. 166–170.

[169] Marlis Ortel and Veit Wagner. "Leidenfrost temperature related CVD-like growth mechanism in ZnO-TFTs deposited by pulsed spray pyrolysis". *Journal of crystal growth* 363 (2013), pp. 185–189.

[170] Adelmo Ortiz-Conde et al. "A review of recent MOSFET threshold voltage extraction methods". *Microelectronics Reliability* 42.4-5 (2002), pp. 583–596.

[171] Shunji Ozaki, Takehito Mishima, and Sadao Adachi. "Photoreflectance spectroscopy of ZnO for ordinary and extraordinary rays". *Japanese journal of applied physics* 42 (2003), p. 5465.

[172] Ü Özgür, V Avrutin, and H Morkoç. "Zinc oxide materials and devices grown by MBE". *Molecular Beam Epitaxy*. Elsevier, 2013, pp. 369–416.

[173] Ü Özgür et al. "A comprehensive review of ZnO materials and devices". *Journal of applied physics* 98.4 (2005), p. 041301.

[174] Ümit Özgür, Vitaliy Avrutin, and Hadis Morkoç. "Zinc oxide materials and devices grown by molecular beam epitaxy". *Molecular Beam Epitaxy*. Elsevier, 2018, pp. 343–375.

[175] Jacques I Pankove. *Optical processes in semiconductors*. Courier Corporation, 1975.

[176] CH Park, SB Zhang, and Su-Huai Wei. "Origin of p-type doping difficulty in ZnO: The impurity perspective". *Physical Review B* 66.7 (2002), p. 073202.

[177] Si Yun Park et al. "Aqueous zinc ammine complex for solution-processed ZnO semiconductors in thin film transistors". *RSC Advances* 4.22 (2014), pp. 11295–11299.

[178] Sungmee Park and Sundaresan Jayaraman. "Smart textiles: Wearable electronic systems". *MRS bulletin* 28.8 (2003), pp. 585–591.

[179] R Pässler. "Dispersion-related assessments of temperature dependences for the fundamental band gap of hexagonal GaN". *Journal of Applied Physics* 90.8 (2001), pp. 3956–3964.

[180] Leo J van der Pauw. "A method of measuring the resistivity and Hall coefficient on lamellae of arbitrary shape". *Philips technical review* 20 (1958), pp. 220–224.

[181] Stephen J Pearton, James W Corbett, and Michael Stavola. *Hydrogen in crystalline semiconductors*. Vol. 16. Springer Science & Business Media, 2013.

[182] Luisa Petti et al. "Metal oxide semiconductor thin-film transistors for flexible electronics". *Applied Physics Reviews* 3.2 (2016), p. 021303.

[183] RC Rai et al. "Elevated temperature dependence of energy band gap of ZnO thin films grown by e-beam deposition". *Journal of Applied Physics* 111.7 (2012), p. 073511.

[184] AP Rambu et al. "Influence of In doping on electro-optical properties of ZnO films". *Bulletin of materials science* 36.2 (2013), pp. 231–237.

[185] MS Ramachandra Rao and Tatsuo Okada. *ZnO nanocrystals and allied materials*. Vol. 180. Springer, 2013.

[186] M Raposo, Q Ferreira, and PA Ribeiro. "A guide for atomic force microscopy analysis of soft-condensed matter". *Modern research and educational topics in microscopy* 1 (2007), pp. 758–769.

[187] DC Reynolds et al. "Valence-band ordering in ZnO". *Physical Review B* 60.4 (1999), p. 2340.

[188] KD Rogers and P Daniels. "An X-ray diffraction study of the effects of heat treatment on bone mineral microstructure". *Biomaterials* 23.12 (2002), pp. 2577–2585.

[189] JF Rommeluere et al. "Electrical activity of nitrogen acceptors in ZnO films grown by metalorganic vapor phase epitaxy". *Applied physics letters* 83.2 (2003), pp. 287–289.

[190] U Rössler. "Energy bands of hexagonal II-VI semiconductors". *Physical Review* 184.3 (1969), p. 733.

[191] L Rozenberg. *Physical principles of ultrasonic technology*. Vol. 1. Springer Science & Business Media, 2013.

[192] Georg Rupprecht. "Untersuchungen der elektrischen und lichtelektrischen Leitfähigkeit dünner Indiumoxydschichten". *Zeitschrift für Physik A Hadrons and Nuclei* 139.5 (1954), pp. 504–517.

[193] PP Sahay. "Zinc oxide thin film gas sensor for detection of acetone". *Journal of Materials Science* 40.16 (2005), pp. 4383–4385.

[194] Masaru Saito and Shinobu Fujihara. "Large photocurrent generation in dye-sensitized ZnO solar cells". *Energy & Environmental Science* 1.2 (2008), pp. 280–283.

[195] N Samaele, P Amornpitoksuk, and S Suwanboon. "Effect of pH on the morphology and optical properties of modified ZnO particles by SDS via a precipitation method". *Powder Technology* 203.2 (2010), pp. 243–247.

[196] Prashant K Sarswat and Michael L Free. "A study of energy band gap versus temperature for Cu2ZnSnS4 thin films". *Physica B: Condensed Matter* 407.1 (2012), pp. 108–111.

[197] M Schirra et al. "Stacking fault related 3.31- eV luminescence at 130-meV acceptors in zinc oxide". *Physical Review B* 77.12 (2008), p. 125215.

[198] Ulrich Schwarz-Schampera and Peter M Herzig. "Technological applications and consumption of indium by industries". *Indium*. Springer, 2002, pp. 167–173.

[199] Krishna Seshan. *Handbook of thin film deposition*. William Andrew, 2012.

[200] Takao Shimizu and Hiroshi Funakubo. "Epitaxial Growth of Doped HfO2 Ferroelectric Materials". *Ferroelectricity in Doped Hafnium Oxide: Materials, Properties and Devices*. Elsevier, 2019, pp. 173–192.

[201] Takahiro Shirahata et al. "Transparent conductive zinc-oxide-based films grown at low temperature by mist chemical vapor deposition". *Thin Solid Films* 597 (2015), pp. 30–38.

[202] Mandeep Singh et al. "Bio-sorbable, liquid electrolyte gated thin-film transistor based on a solution-processed zinc oxide layer". *Faraday discussions* 174 (2014), pp. 383–398.

[203] Takao Someya et al. "Conformable, flexible, large-area networks of pressure and thermal sensors with organic transistor active matrixes". *Proceedings of the National Academy of Sciences of the United States of America* 102.35 (2005), pp. 12321–12325.

[204] V Srikant and DR Clarke. "Optical absorption edge of ZnO thin films: the effect of substrate". *Journal of applied physics* 81.9 (1997), pp. 6357–6364.

[205] Yuri M Strzhemechny et al. "Remote hydrogen plasma doping of single crystal ZnO". *Applied physics letters* 84.14 (2004), pp. 2545–2547.

[206] SA Studenikin, Nickolay Golego, and Michael Cocivera. "Fabrication of green and orange photoluminescent, undoped ZnO films using spray pyrolysis". *Journal of Applied Physics* 84.4 (1998), pp. 2287–2294.

[207] XW Sun and HS Kwok. "Optical properties of epitaxially grown zinc oxide films on sapphire by pulsed laser deposition". *Journal of applied physics* 86.1 (1999), pp. 408–411.

[208] Yashu Swami and Sanjeev Rai. "Modeling, simulation, and analysis of novel threshold voltage definition for nano-MOSFET". *Journal of Nanotechnology* 2017 (2017).

[209] R Swanepoel. "Determination of the thickness and optical constants of amorphous silicon". *Journal of Physics E: Scientific Instruments* 16.12 (1983), p. 1214.

[210] Simon M Sze and Kwok K Ng. *Physics of semiconductor devices*. John wiley & sons, 2006.

[211] Simon Min Sze. *Semiconductor devices: physics and technology*. John wiley & sons, 2008.

[212] Kun Tang et al. "Optical fingerprints of donors and acceptors in high-quality NH 3-doped ZnO films". *Optical Materials Express* 7.4 (2017), pp. 1169–1179.

[213] J Tauc, Radu Grigorovici, and Anina Vancu. "Optical properties and electronic structure of amorphous germanium". *physica status solidi (b)* 15.2 (1966), pp. 627–637.

[214] Carl V Thompson. "Structure evolution during processing of polycrystalline films". *Annual review of materials science* 30.1 (2000), pp. 159–190.

[215] Michael N Topp. "Ultrasonic atomization-a photographic study of the mechanism of disintegration". *Journal of Aerosol Science* 4.1 (1973), pp. 17–25.

[216] Sylvain Tricot et al. "Epitaxial ZnO thin films grown by pulsed electron beam deposition". *Surface Science* 604.21-22 (2010), pp. 2024–2030.

[217] Atsushi Tsukazaki et al. "Repeated temperature modulation epitaxy for p-type doping and light-emitting diode based on ZnO". *Nature materials* 4.1 (2005), p. 42.

[218] Gary Chandler Turner. "Zinc Oxide MESFET Transistors". MSc Thesis. University of Canterbury.

[219] Kazuyuki Uno, Yuichiro Yamasaki, and Ichiro Tanaka. "Growth mechanisms of zinc oxide and zinc sulfide films by mist chemical vapor deposition". *Applied Physics Express* 10.1 (2016), p. 015502.

[220] Franz Urbach. "The long-wavelength edge of photographic sensitivity and of the electronic absorption of solids". *Physical Review* 92.5 (1953), p. 1324.

[221] GG Valle et al. "Transparent and conductive ZnO: Al thin films prepared by sol-gel dip-coating". *Journal of the European Ceramic Society* 24.6 (2004), pp. 1009–1013.

[222] Yatendra Pal Varshni. "Temperature dependence of the energy gap in semiconductors". *physica* 34.1 (1967), pp. 149–154.

[223] Dirk Vogel, Peter Krüger, and Johannes Pollmann. "Self-interaction and relaxation-corrected pseudopotentials for II-VI semiconductors". *Physical Review B* 54.8 (1996), p. 5495.

[224] Sofie Vogt, Holger von Wenckstern, and Marius Grundmann. "MESFETs and inverters based on amorphous zinc-tin-oxide thin films prepared at room temperature". *Applied Physics Letters* 113.13 (2018), p. 133501.

[225] I Volintiru et al. "Nitrogen incorporation during metal organic chemical vapor deposition of ZnO films using a remote Ar/ N 2 plasma". *Applied physics letters* 89.2 (2006), p. 022110.

[226] MS Wagh et al. "Modified zinc oxide thick film resistors as NH3 gas sensor". *Sensors and Actuators B: Chemical* 115.1 (2006), pp. 128–133.

[227] Igori Wallace et al. "Synthesis and Characterization of Zinc Oxide (ZnO) Nanowire". *Journal of Nanomedicine & Nanotechnology* 6.5 (2015), p. 1.

[228] Chris G Van de Walle. "Hydrogen as a cause of doping in zinc oxide". *Physical review letters* 85.5 (2000), p. 1012.

[229] Lijun Wang and NC Giles. "Temperature dependence of the free-exciton transition energy in zinc oxide by photoluminescence excitation spectroscopy". *Journal of Applied Physics* 94.2 (2003), pp. 973–978.

[230] Xu Wang et al. "Energy band bowing parameter in MgZnO alloys". *Applied Physics Letters* 107.2 (2015), p. 022111.

[231] Xudong Wang, Jinhui Song, and Zhong Lin Wang. "Nanowire and nanobelt arrays of zinc oxide from synthesis to properties and to novel devices". *Journal of Materials Chemistry* 17.8 (2007), pp. 711–720.

[232] Yao Wang et al. "Optical modulation of persistent photoconductivity in ZnO nanowires". *Applied Physics Letters* 98.20 (2011), p. 203108.

[233] Yi-Dong Wang and Jun Chen. "Modeling capacitance–voltage characteristic of TiW/p-InP Schottky barrier diode". *Chinese Physics B* 27.9 (2018), p. 097203.

[234] Yu-Lin Wang et al. "Room temperature deposited indium zinc oxide thin film transistors". *Applied physics letters* 90.23 (2007), p. 232103.

[235] Yuchao Wang et al. "Well-controlled wet etching of ZnO films using hydrogen peroxide solution". *Applied Surface Science* 292 (2014), pp. 34–38.

[236] Zhong Lin Wang. "Zinc oxide nanostructures: growth, properties and applications". *Journal of Physics: Condensed Matter* 16.25 (2004), R829.

[237] *What is DC Sputtering?* Nov. 26, 2016. URL: http://www.semicore.com/news/94-what-is-dc-sputtering.

[238] Matthew David Whiteside. "Characterization and Stability of MESFETs Fabricated on Amorphous Indium Gallium Zinc Oxide". MSc Thesis. University of Canterbury.

[239] *Wide Bandgap Semiconductors Go Beyond Silicon in Power, RF, LED Lighting, and Optoelectronics*. URL: https://www.mouser.com/applications/wide-bandgap-beyond-silicon/.

[240] James P Wolfe. "Thermodynamics of excitons in semiconductors". *PhT* 35.3 (1982), pp. 46–54.

[241] Ping Wu et al. "Instability induced by ultraviolet light in ZnO thin-film transistors". *IEEE Transactions on Electron Devices* 61.5 (2014), pp. 1431–1435.

[242] Yong Xie et al. "Enforced c-axis growth of ZnO epitaxial chemical vapor deposition films on a-plane sapphire". *Applied Physics Letters* 100.18 (2012), p. 182101.

[243] Xia Yan, Selvaraj Venkataraj, and Armin G Aberle. "Modified surface texturing of aluminium-doped zinc oxide (AZO) transparent conductive oxides for thin-film silicon solar cells". *Energy Procedia* 33 (2013), pp. 157–165.

[244] G-C Yi et al. "ZnO nanorods and their heterostructures for electrical and optical nanodevice applications" (2016).

[245] Akihiko Yoshikawa, Hiroyuki Matsunami, and Yasushi Nanishi. "Development and applications of wide bandgap semiconductors". *Wide Bandgap Semiconductors*. Springer, 2007, pp. 1–24.

[246] J Zhang et al. "Evolution of electrical performance of ZnO-based thin-film transistors by low temperature annealing". *AIP Advances* 2.2 (2012), p. 022118.

[247] JP Zhang et al. "Characterization of ZnO: N films prepared by annealing sputtered zinc oxynitride films at different temperatures". *Journal of Applied Physics* 102.11 (2007), p. 114903.

[248] Liang Zhang et al. "Enhanced performances of ZnO-TFT by improving surface properties of channel layer". *Solid State Communications* 146.9-10 (2008), pp. 387–390.

[249] Lirong Zhang et al. "Research progress on flexible oxide-based thin film transistors". *Applied Sciences* 9.4 (2019), p. 773.

[250] SB Zhang, S-H Wei, and Alex Zunger. "Intrinsic n-type versus p-type doping asymmetry and the defect physics of ZnO". *Physical Review B* 63.7 (2001), p. 075205.

[251] Xinan Zhang et al. "Analysis of the electrical characteristics of the Ag/ZnO Schottky barrier diodes on F-doped SnO2 glass substrates by pulsed laser deposition". *Microelectronic Engineering* 93 (2012), pp. 5–9.

[252] Jie Zhao et al. "ZnO thin films on Si (1 1 1) grown by pulsed laser deposition from metallic Zn target". *Applied Surface Science* 253.2 (2006), pp. 841–845.

[253] Jun-Liang Zhao et al. "Structural, optical and electrical properties of ZnO films grown by pulsed laser deposition (PLD)". *Journal of Crystal Growth* 276.3-4 (2005), pp. 507–512.